

SX-A Family FPGAs

Leading-Edge Performance

- 250 MHz System Performance
- 350 MHz Internal Performance
- 3.8 ns Clock-to-Out (Pad-to-Pad)

Specifications

- 12,000 to 108,000 Available System Gates
- Up to 360 User-Programmable I/O Pins
- Up to 2,012 Dedicated Flip-Flops
- 0.22 μ /0.25 μ CMOS Process Technology

Features

- Hot-Swap Compliant I/Os
- Power-up/down Friendly (No Sequencing Required for Supply Voltages)
- 66 MHz PCI Compliant
- Single-Chip Solution
- Nonvolatile

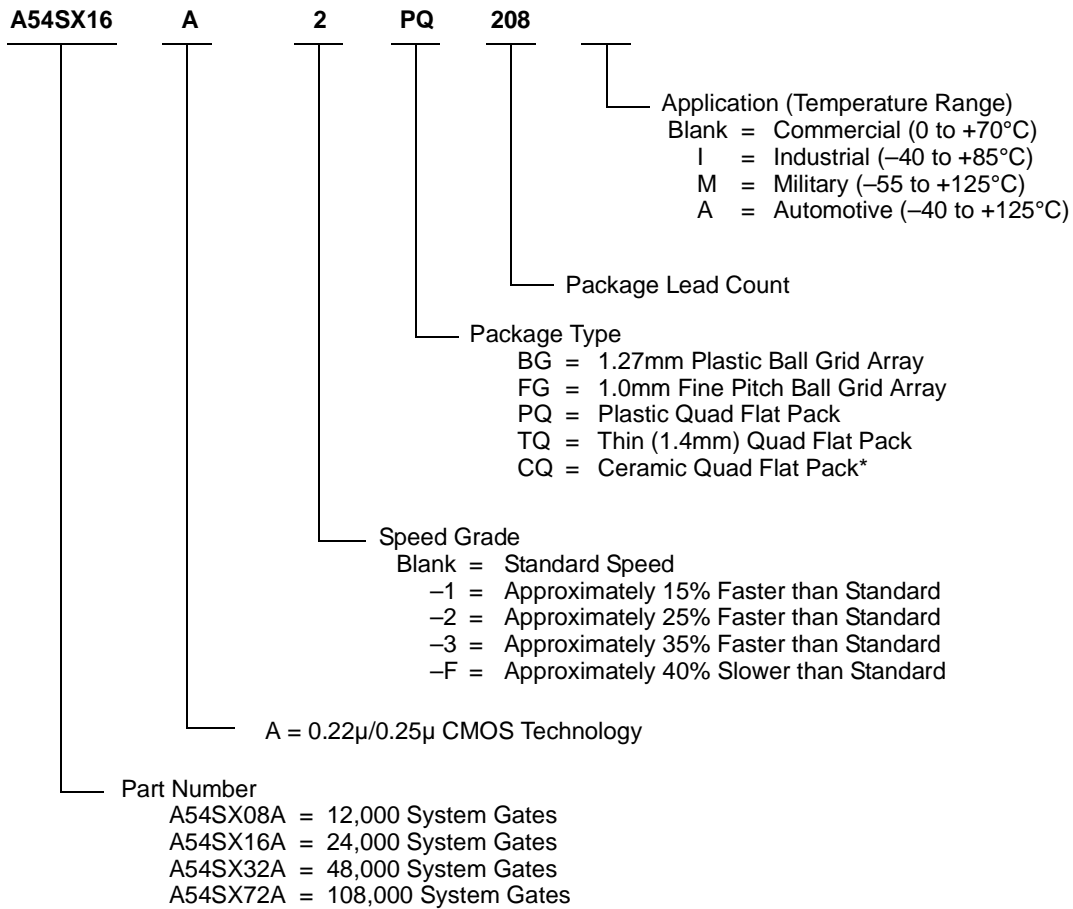
- Configurable I/O Support for 3.3V/5V PCI, 5V TTL, 3.3V LVTTTL, 2.5V LVCMOS2
- 2.5V, 3.3V, and 5V Mixed-Voltage Operation with 5V Input Tolerance and 5V Drive Strength
- Devices Support Multiple Temperature Grades
- Configurable Weak-Resistor Pull-up or Pull-down for Outputs at Power-up
- Individual Output Slew Rate Control
- Up to 100% Resource Utilization and 100% Pin Locking
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Boundary Scan Testing in Compliance with IEEE Standard 1149.1 (JTAG)
- Actel's Secure Programming Technology with FuseLock™ Prevents Reverse Engineering and Design Theft

SX-A Product Profile

Device	A54SX08A	A54SX16A	A54SX32A	A54SX72A
Capacity				
Typical Gates	8,000	16,000	32,000	72,000
System Gates	12,000	24,000	48,000	108,000
Logic Modules	768	1,452	2,880	6,036
Combinatorial Cells	512	924	1,800	4,024
Register Cells				
Dedicated Flip-Flops	256	528	1,080	2,012
Maximum Flip-Flops	512	990	1,980	4,024
Maximum User I/Os	130	180	249	360
Global Clocks	3	3	3	3
Quadrant Clocks	0	0	0	4
Boundary Scan Testing	Yes	Yes	Yes	Yes
3.3V/5V PCI	Yes	Yes	Yes	Yes
Clock-to-Out	4.2 ns	4.6 ns	4.7 ns	5.8 ns
Input Set-Up (External)	0 ns	0 ns	0 ns	0 ns
Speed Grades	-F, Std, -1, -2, -3	-F, Std, -1, -2, -3	-F, Std, -1, -2, -3	-F, Std, -1, -2, -3
Temperature Grades	C, I, A	C, I, M, A	C, I, M, A	C, I, M, A
Package (by pin count)				
PQFP	208	208	208	208
TQFP	100, 144	100, 144	100, 144, 176	—
PBGA	—	—	329	—
FBGA	144	144, 256	144, 256, 484	256, 484
CQFP*	—	—	208, 256	208, 256

Note: For more information about the CQFP package options, refer to the HiRel SX-A datasheet at: www.actel.com/documents/HRSXADS.pdf

Ordering Information



*For more information about the CQFP package options, refer to the HiRel SX-A datasheet at: www.actel.com/documents/HRSXADS.pdf

Plastic Device Resources

Device	User I/Os (including clock buffers)							
	PQFP 208-Pin	TQFP 100-Pin	TQFP 144-Pin	TQFP 176-Pin	PBGA 329-Pin	FBGA 144-Pin	FBGA 256-Pin	FBGA 484-Pin
A54SX08A	130	81	113	—	—	111	—	—
A54SX16A	175	81	113	—	—	111	180	—
A54SX32A	174	81	113	147	249	111	203	249
A54SX72A	171	—	—	—	—	—	203	360

Contact your Actel sales representative for product availability.

Package Definitions

PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, PBGA = 1.27mm Plastic Ball Grid Array, FBGA = 1.0mm Fine Pitch Ball Grid Array

Product Plan

	Speed Grade**					Application			
	-F	Std	-1	-2	-3	C	I†	M*	A
A54SX08A Device									
100-Pin Thin Quad Flat Pack (TQFP)	✓	✓	✓	✓	✓	✓	✓	✓	✓
144-Pin Thin Quad Flat Pack (TQFP)	✓	✓	✓	✓	✓	✓	✓	✓	✓
208-Pin Plastic Quad Flat Pack (PQFP)	✓	✓	✓	✓	✓	✓	✓	✓	✓
144-Pin Fine Pitch Ball Grid Array (FBGA)	✓	✓	✓	✓	✓	✓	✓	✓	✓
A54SX16A Device									
100-Pin Thin Quad Flat Pack (TQFP)	✓	✓	✓	✓	✓	✓	✓	✓	✓
144-Pin Thin Quad Flat Pack (TQFP)	✓	✓	✓	✓	✓	✓	✓	✓	✓
208-Pin Plastic Quad Flat Pack (PQFP)	✓	✓	✓	✓	✓	✓	✓	✓	✓
144-Pin Fine Pitch Ball Grid Array (FBGA)	✓	✓	✓	✓	✓	✓	✓	✓	✓
256-Pin Fine Pitch Ball Grid Array (FBGA)	✓	✓	✓	✓	✓	✓	✓	✓	✓
A54SX32A Device									
100-Pin Thin Quad Flat Pack (TQFP)	✓	✓	✓	✓	✓	✓	✓	✓	✓
144-Pin Thin Quad Flat Pack (TQFP)	✓	✓	✓	✓	✓	✓	✓	✓	✓
176-Pin Thin Quad Flat Pack (TQFP)	✓	✓	✓	✓	✓	✓	✓	✓	-
208-Pin Plastic Quad Flat Pack (PQFP)	✓	✓	✓	✓	✓	✓	✓	✓	✓
208-Pin Ceramic Quad Flat Pack (CQFP)*	✓	✓	✓	✓	✓	✓	✓	✓	-
256-Pin Ceramic Quad Flat Pack (CQFP)*	✓	✓	✓	✓	✓	✓	✓	✓	-
144-Pin Fine Pitch Ball Grid Array (FBGA)	✓	✓	✓	✓	✓	✓	✓	✓	✓
256-Pin Fine Pitch Ball Grid Array (FBGA)	✓	✓	✓	✓	✓	✓	✓	✓	✓
329-Pin Plastic Ball Grid Array (PBGA)	✓	✓	✓	✓	✓	✓	✓	✓	-
484-Pin Fine Pitch Ball Grid Array (FBGA)	✓	✓	✓	✓	✓	✓	✓	✓	-
A54SX72A Device									
208-Pin Plastic Quad Flat Pack (PQFP)	✓	✓	✓	✓	✓	✓	✓	✓	✓
208-Pin Ceramic Quad Flat Pack (CQFP)*	✓	✓	✓	✓	✓	✓	✓	✓	-
256-Pin Ceramic Quad Flat Pack (CQFP)*	✓	✓	✓	✓	✓	✓	✓	✓	-
256-Pin Fine Pitch Ball Grid Array (FBGA)	✓	✓	✓	✓	✓	✓	✓	✓	✓
484-Pin Fine Pitch Ball Grid Array (FBGA)	✓	✓	✓	✓	✓	✓	✓	✓	✓

Contact your Actel sales representative for product availability.

*For more information about the CQFP package options, refer to the HiRel SX-A datasheet at: www.actel.com/documents/HRSXADS.pdf

Applications: C = Commercial Availability: ✓ = Available **Speed Grade: -1 = Approx. 15% faster than Standard
 I = Industrial -2 = Approx. 25% faster than Standard
 M = Military -3 = Approx. 35% faster than Standard
 A = Automotive

-F = Approx. 40% slower than Standard

† Only Std, -1, -2 Speed Grade

• Only Std, -1 Speed Grade

General Description

Actel's SX-A family of FPGAs features a sea-of-modules architecture that delivers high device performance. SX-A devices simplify design time, enable dramatic reductions in design costs and power consumption, and further decrease time-to-market for performance-intensive applications.

Actel's SX-A architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. The routing and interconnect resources are in the metal layers above the logic modules, providing optimal use of silicon. This enables the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or "sea-of-modules"), which reduces the distance signals have to travel between logic modules. To minimize signal propagation delay, SX-A devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (90 percent of connections typically use only three or fewer antifuses). The unique local and general routing structure featured in SX-A devices gives fast and predictable performance, allows 100% pin-locking with full logic

utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with minimum effort.

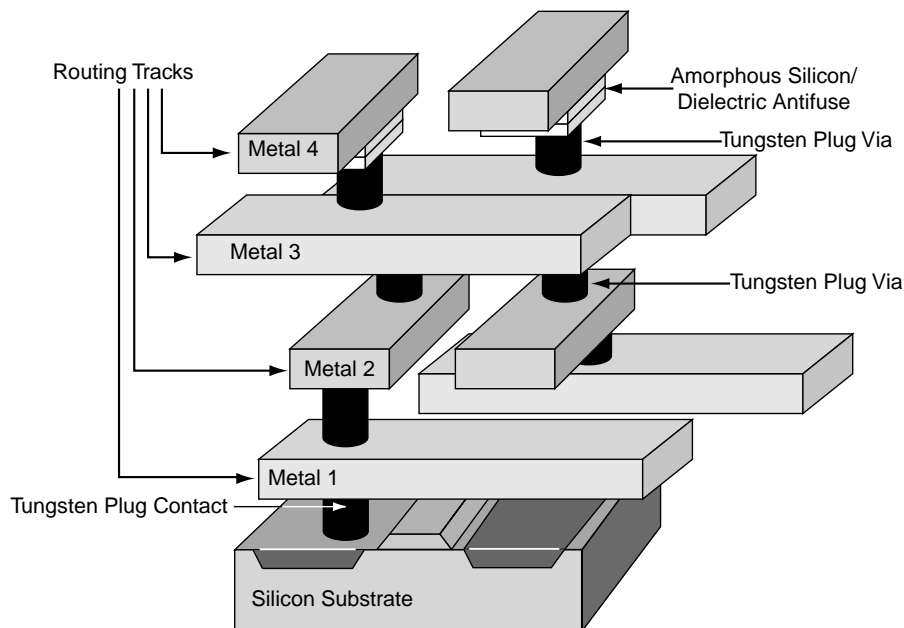
Further complementing SX-A's flexible routing structure is a hardwired, constantly loaded clock network that has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input set-up times. SX-A devices have easy-to-use I/O cells that do not require HDL instantiation, facilitating design re-use and reducing design and verification time.

SX-A Family Architecture

The SX-A family architecture was designed to satisfy performance and integration requirements for production-volume designs in a broad range of applications.

Programmable Interconnect Element

The SX-A family provides efficient use of silicon by locating the routing interconnect resources between the top two metal layers (Figure 1). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.



Note: A54SX72A has four layers of metal with the antifuse between Metal 3 and Metal 4. A54SX08A, A54SX16A, and A54SX32A have three layers of metal with antifuse between Metal 2 and Metal 3.

Figure 1 • SX-A Family Interconnect Elements

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX-A family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and since SX-A is a nonvolatile, single-chip solution, there is no configuration bitstream to intercept.

Additionally, the interconnect (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

Logic Module Design

The SX-A family architecture is described as a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. Actel's SX-A family provides two types of logic

modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX-A FPGA. The clock source for the R-cell can be chosen from either the hardwired clock, the routed clocks, or internal logic.

The C-cell implements a range of combinatorial functions of up to five inputs (Figure 3 on page 6). Inclusion of the DB input and its associated inverter function increases the number of combinatorial functions that can be implemented in a single module from 800 options (as in previous architectures) to more than 4,000 in the SX-A architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 1.9 ns propagation delays. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.

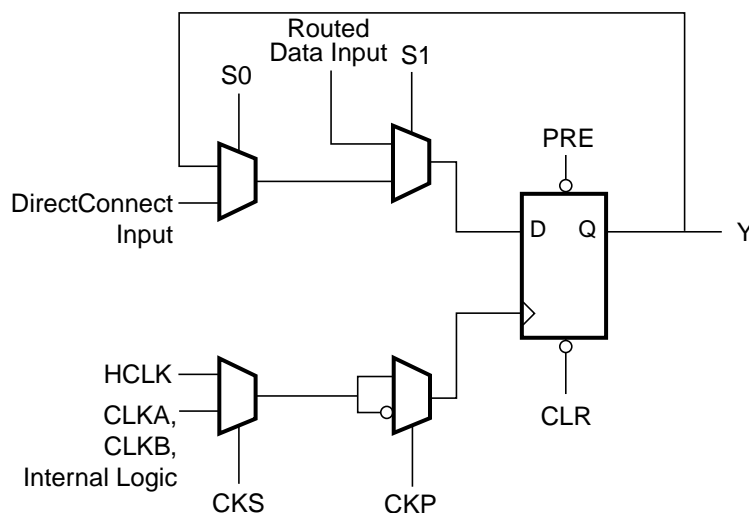


Figure 2 • R-Cell

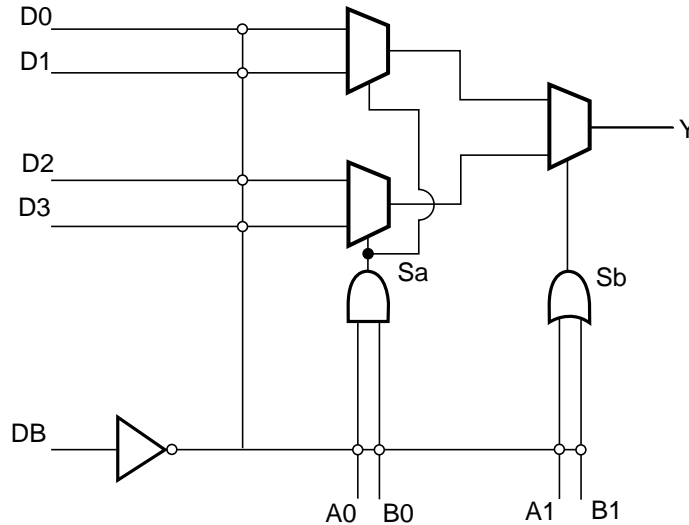


Figure 3 • C-Cell

Chip Architecture

The SX-A family's chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called Clusters. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into SuperClusters (Figure 4 on page 7). SuperCluster 1 is a two-wide grouping of Type 1 Clusters. SuperCluster 2 is a two-wide group containing one Type 1 Cluster and one Type 2 Cluster. SX-A devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 5 and Figure 6 on page 8). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum pin-to-pin propagation time of 0.3 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. Actel's segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100% automatic place-and-route software to minimize signal propagation delays.

Clock Resources

Actel's high-drive routing structure provides three clock networks (Table 1). The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select MUX in each R-cell. HCLK cannot be connected to combinatorial logic. This provides a fast propagation path for the clock signal, enabling the 3.8 ns clock-to-out (pad-to-pad) performance of the SX-A devices. The hardwired clock is tuned to provide clock skew less than 0.3 ns worst case. If not used, this pin must be set as LOW or HIGH on the board. It must not be left floating. Figure 7 describes the clock circuit used for the constant load HCLK. Upon power-up of the SX-A device, four clock pulses must be detected on HCLK before the clock signal will be propagated to registers in the design.

Two additional clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX-A device. CLKA and CLKB may be connected to sequential cells or to combinatorial logic. If

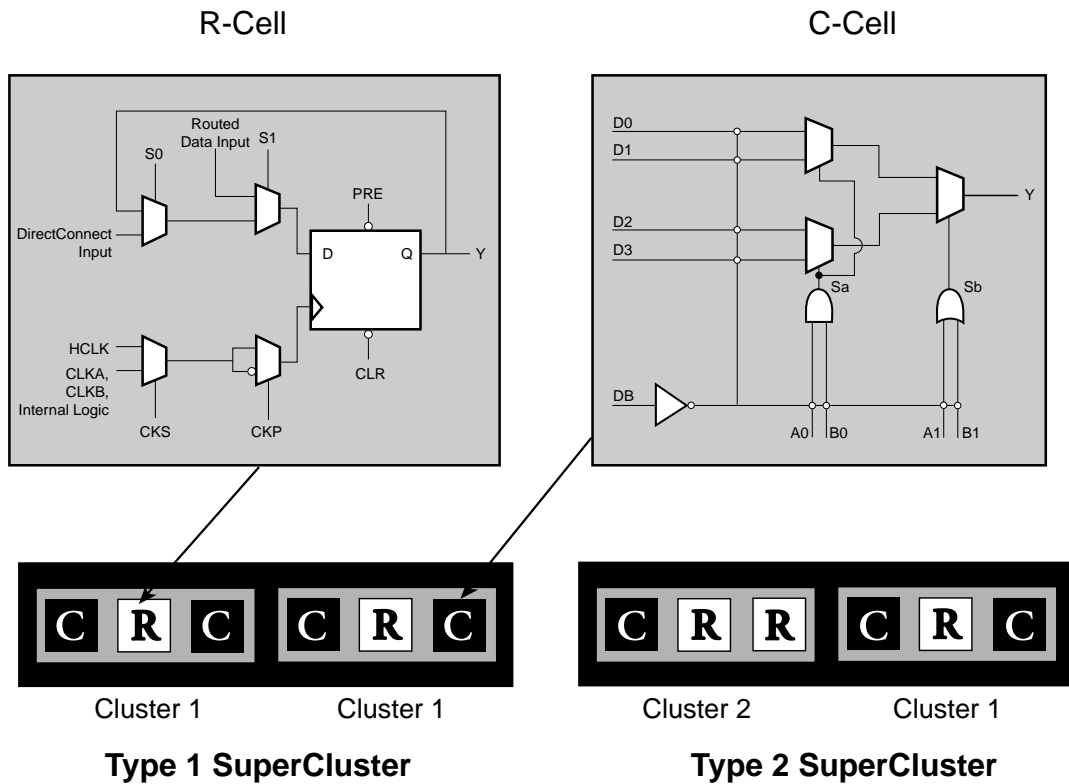


Figure 4 • Cluster Organization

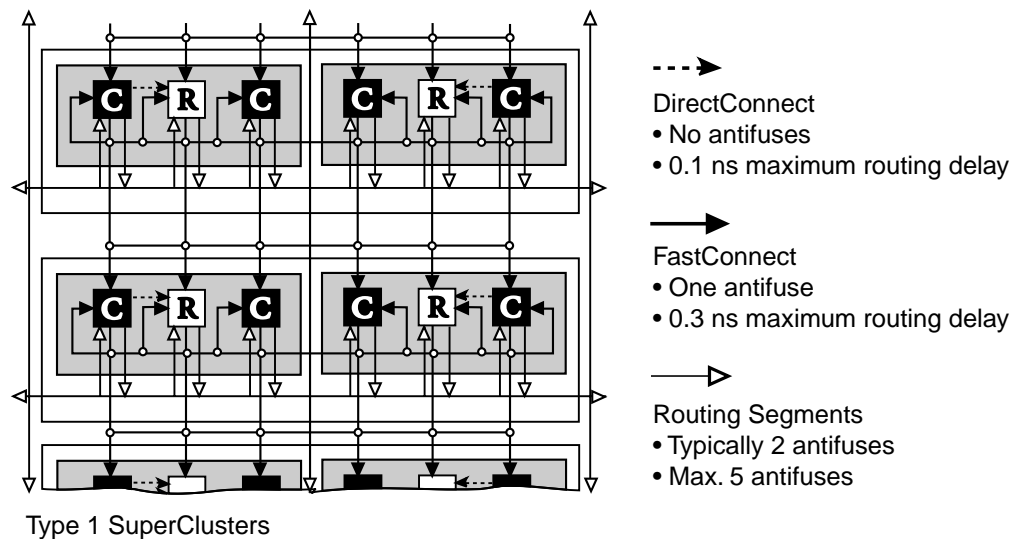


Figure 5 • DirectConnect and FastConnect for Type 1 SuperClusters

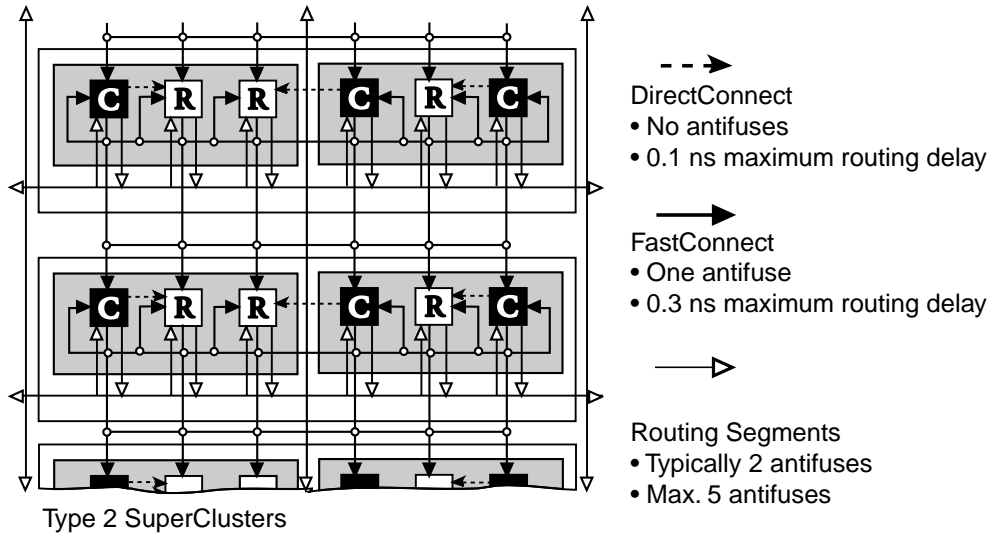


Figure 6 • DirectConnect and FastConnect for Type 2 SuperClusters

CLKA or CLKB pins are not used or sourced from signals, then these pins must be set as LOW or HIGH on the board. They must not be left floating (except in the A54SX72A where these clocks can be configured as regular I/Os and can float). Figure 8 describes the CLKA and CLKB circuit used in SX-A devices with the exception of A54SX72A.

In addition, the A54SX72A device provides four quadrant clocks (QCLKA, QCLKB, QCLKC, QCLKD – corresponding to bottom-left, bottom-right, top-left, and top-right locations on the die, respectively), which can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to a quarter of the chip,

or they can be grouped together to drive multiple quadrants. If QCLKs are not used as quadrant clocks, they will behave as regular I/Os. Bidirectional clock buffers are also available on the A54SX72A. The CLKA, CLKB, and QCLK circuits for A54SX72A are shown in Figure 9 on page 9. Note that bidirectional clock buffers are only available in A54SX72A. For more information, refer to the “Pin Description” section on page 53.

For more information on how to use quadrant clocks in the A54SX72A device, refer to the *Global Clock Networks in Actel’s Antifuse Devices* and *Using A54SX72A and RT54SX72S Quadrant Clocks* application notes.

Table 1 • SX-A Clock Resources

	A54SX08A	A54SX16A	A54SX32A	A54SX72A
Routed Clocks (CLKA, CLKB)	2	2	2	2
Hardwired Clocks (HCLK)	1	1	1	1
Quadrant Clocks (QCLKA, QCLKB, QCLKC, QCLKD)	0	0	0	4

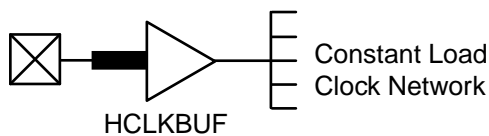
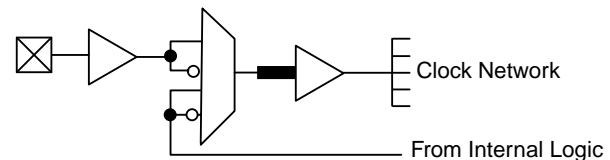


Figure 7 • SX-A HCLK Clock Pad



CLKBUF
CLKBUF1
CLKINT
CLKINT1

Note: This does not include the clock pad for HiRel A54SX72A.

Figure 8 • SX-A Routed Clock Structure

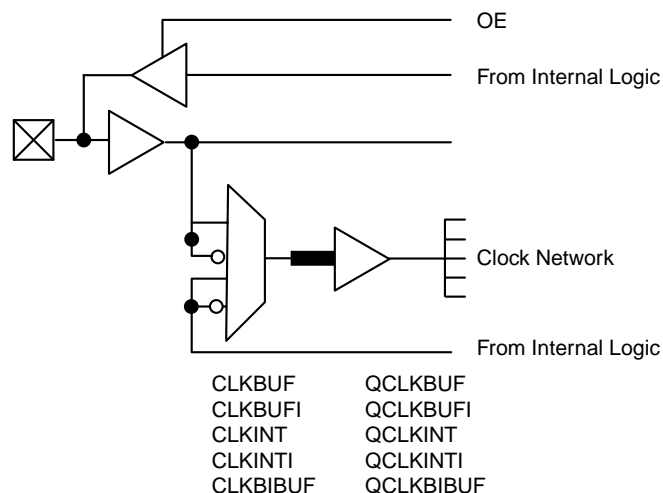


Figure 9 • A54SX72A Routed Clock and QClock Structure

Other Architectural Features

Technology

Actel's SX-A family is implemented on a high-voltage, twin-well CMOS process using 0.22 μ /0.25 μ design rules. The metal-to-metal antifuse is comprised of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ("on" state) resistance of 25 Ω with capacitance of 1.0 fF for low signal impedance.

Performance

The combination of architectural features described above enables SX-A devices to operate with internal clock frequencies of 350 MHz, enabling very fast execution of even complex logic functions. Thus, the SX-A family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can be integrated into an SX-A device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

User Security

The Actel FuseLock advantage ensures that unauthorized users will not be able to read back the contents of an Actel antifuse FPGA. In addition to the inherent strengths of the architecture, special security fuses that prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located such that they cannot be accessed or bypassed without destroying the rest of the device, making both invasive and more-subtle noninvasive attacks ineffective against Actel antifuse FPGAs.

Look for this symbol to ensure your valuable IP is secure.



For more information, refer to Actel's *Implementation of Security in Actel Antifuse FPGAs* application note.

I/O Modules

Each user I/O on an SX-A device can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards can be set for individual pins, though this is only allowed with the same voltage as the input. These I/Os, combined with array registers, can achieve clock-to-output-pad timing as fast as 3.8 ns even without the dedicated I/O registers. In most FPGAs, I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in SX-A FPGAs. Fast pin-to-pin timing ensures that the device is able to interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time. All unused I/Os are configured as tristate outputs by Actel's Designer software, for maximum flexibility when designing new boards or migrating existing designs.

SX-A inputs should be driven by high-speed push-pull devices with a low-resistance pull-up device. If the input voltage is greater than V_{CCI} and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the SX-A I/O may create a voltage divider. This voltage divider could pull the input voltage below specification for some devices connected to the driver. A logic '1' may not be correctly presented in this case. For example, if an open

drain driver is used with a pull-up resistor to 5V to provide the logic '1' input, and V_{CCI} is set to 3.3V on the SX-A device, the input signal may be pulled down by the SX-A input.

Each I/O module has an available power-up resistor of approximately 50k Ω that can configure the I/O in a known state during power-up. Just slightly before V_{CCA} reaches 2.5V, the resistors are disabled, so the I/Os will be controlled by user logic. See [Table 2](#) and [Table 3](#) for more information concerning available I/O features.

Hot Swapping

SX-A I/Os can be configured to be hot-swappable in compliance with the Compact PCI (5.0V) Specification. However, note that 3.3V PCI device is not hot swappable.

During power-up/down (or partial up/down), all I/Os are tristated. V_{CCA} and V_{CCI} do not have to be stable during power-up/down. After the SX-A device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions are reached. [Table 4](#) summarizes the V_{CCA} voltage at which the I/Os behave according to the user's design for an SX-A device at room temperature for various ramp-up rates. The data reported assumes a linear ramp-up profile to 2.5V. For more information on power-up and hot-swapping, refer to the application note, *Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications*.

Table 2 • I/O Features

Function	Description
Input Buffer Threshold Selections	<ul style="list-style-type: none"> • 5V PCI, TTL • 3.3V PCI, LVTTTL • 2.5V LVCMOS2
Flexible Output Driver	<ul style="list-style-type: none"> • 5V: PCI, TTL • 3.3V: PCI, LVTTTL • 2.5V: LVCMOS2
Output Buffer	"Hot-Swap" Capability (3.3V PCI is not hot swappable) <ul style="list-style-type: none"> • I/O on an unpowered device does not sink current • Can be used for "cold-sparing" Selectable on an individual I/O basis Individually selectable slew rate, high slew or low slew (The default is high slew rate). The slew is only affected on the falling edge of an output. Rising edges of outputs are not affected.
Power-Up	Individually selectable pull-ups and pull-downs during power-up (default is to power-up in tristate) Enables deterministic power-up of device V_{CCA} and V_{CCI} can be powered in any order

Table 3 • I/O Characteristics for All I/O Configurations

	Hot Swappable	Slew Rate Control	Power-up Resistor
TTL, LVTTTL, LVCMOS2	Yes	Yes. Only affects falling edges of outputs	pull-up or pull-down
3.3V PCI	No	No. High slew rate only	pull-up or pull-down
5V PCI	Yes	No. High slew rate only	pull-up or pull-down

Table 4 • Power-up Time at which I/Os Become Active

Supply Ramp Rate	0.25V/ μ s	0.025V/ μ s	5V/ms	2.5V/ms	0.5V/ms	0.25V/ms	0.1V/ms	0.025V/ms
Units	μ s	μ s	ms	ms	ms	ms	ms	ms
A54SX08A	10	96	0.34	0.65	2.7	5.4	12.9	50.8
A54SX16A	10	100	0.36	0.62	2.5	4.7	11.0	41.6
A54SX32A	10	100	0.46	0.74	2.8	5.2	12.1	47.2
A54SX72A	10	100	0.41	0.67	2.6	5.0	12.1	47.2

Boundary-Scan Testing (BST)

All SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as user I/O in either mode.

Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, users need to reserve the JTAG pins in Actel's Designer software. To reserve the JTAG pins, users can check the "Reserve JTAG" box in "Device Selection Wizard" (Figure 10).

Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, users need to uncheck the "Reserve JTAG" box in "Device Selection Wizard" in Actel's

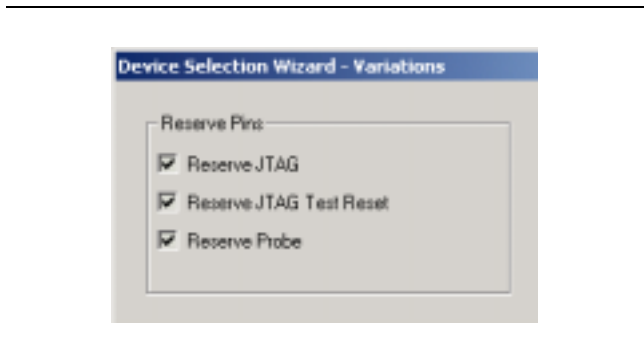


Figure 10 • Device Selection Wizard

Designer software. In Flexible mode, TDI, TCK and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST TAP controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. An external 10K pull-up resistor to V_{CCI} should be placed on the TMS pin to pull it HIGH by default.

Table 5 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 5 • Boundary-Scan Pin Configurations and Functions

Mode	Designer "Reserve JTAG" Selection	TAP Controller State
Dedicated (JTAG)	Checked	Any
Flexible (User I/O)	Unchecked	Test-Logic-Reset
Flexible (JTAG)	Unchecked	Any EXCEPT Test-Logic-Reset

TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the "Reserve JTAG Test Reset" option is selected as shown in Figure 10. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or be driven high.

When the "Reserve JTAG Test Reset" option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

Probing Capabilities

SX-A devices also provide an internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II Diagnostic Hardware is used to control the TDI, TCK, TMS and TDO pins to select the desired nets for debugging. The user assigns the selected internal nets in Actel's Silicon Explorer II software to the PRA/PRB output pins for

observation. Silicon Explorer II automatically places the device into JTAG mode. However, probing functionality is only activated when the TRST pin is driven high or left floating, allowing the internal pull-up resistor to pull TRST HIGH. If the TRST pin is held LOW, the TAP controller remains in the Test-Logic-Reset state so no probing can be performed. However, the user must drive the TRST pin HIGH or allow the internal pull-up resistor to pull TRST HIGH.

When selecting the "Reserve Probe Pin" box as shown in Figure 10, direct the layout tool to reserve the PRA and PRB pins as dedicated outputs for probing. This "reserve" option is merely a guideline. If the designer assigns user I/Os to the PRA and PRB pins and selects the "Reserve Probe Pin" option, Designer Layout will override the "Reserve Probe Pin" option and place the user I/Os on those pins.

To allow probing capabilities, the security fuse must not be programmed. Programming the security fuse disables the probe circuitry. Table 6 summarizes the possible device configurations for probing once the device leaves the "Test-Logic-Reset" JTAG state.

Table 6 • Device Configuration Options for Probe Capability (TRST pin reserved)

JTAG Mode	TRST ¹	Security Fuse Programmed	PRA, PRB ²	TDI, TCK, TDO ²
Dedicated	LOW	No	User I/O ³	Probing Unavailable
Flexible	LOW	No	User I/O ³	User I/O ³
Dedicated	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
Flexible	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
–	–	Yes	Probe Circuit Secured	Probe Circuit Secured

Notes:

1. If the TRST pin is not reserved, the device behaves according to TRST=HIGH as described in the table.
2. Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.
3. If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by the Designer software.

SX-A Probe Circuit Control Pins

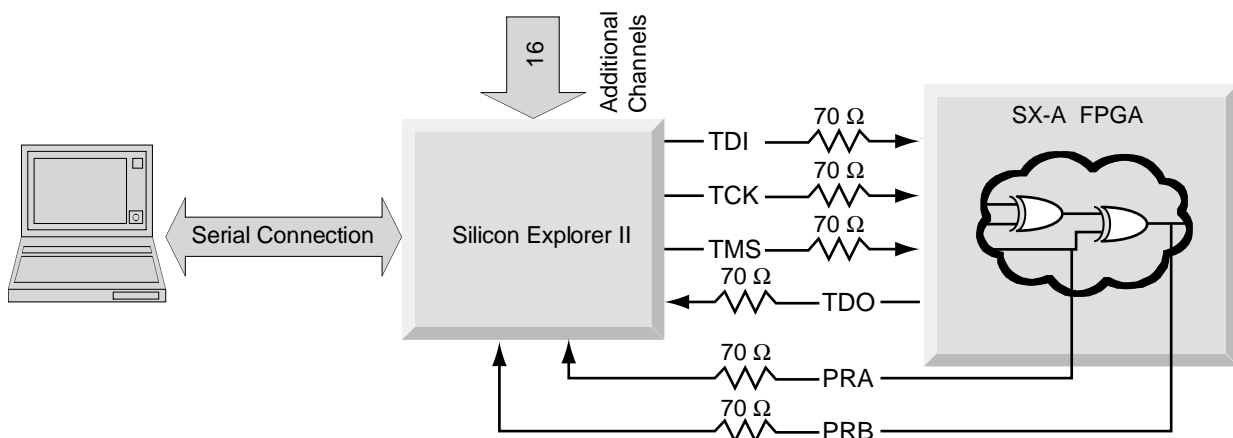
SX-A devices contain internal probing circuitry that provides built-in access to every node in a design, enabling 100% real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy to use integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18 channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary-scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for

verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 11 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

Design Considerations

Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, critical input signals through these pins are not available. In addition, do not program the Security Fuse. Programming the Security Fuse disables the Probe Circuit. Actel recommends that you use a 70Ω series termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.


Figure 11 • Probe Setup

Development Tool Support

The SX-A family of FPGAs is fully supported by both the Actel Libero™ Integrated Design Environment and the Actel Designer FPGA Development Software. Actel's Designer software provides a comprehensive suite of back-end development tools for FPGA development. The Designer software includes timing-driven place and route, a world-class integrated static timing analyzer and constraints editor, and a design netlist schematic viewer.

Libero IDE provides an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Libero IDE includes Synplicity® Synplify for Actel, Mentor Graphics™ ViewDraw for Actel, Actel's own Designer software, Model Technology™ ModelSim HDL Simulator, and SynaptiCAD™ WaveFormer Lite (Figure 12).

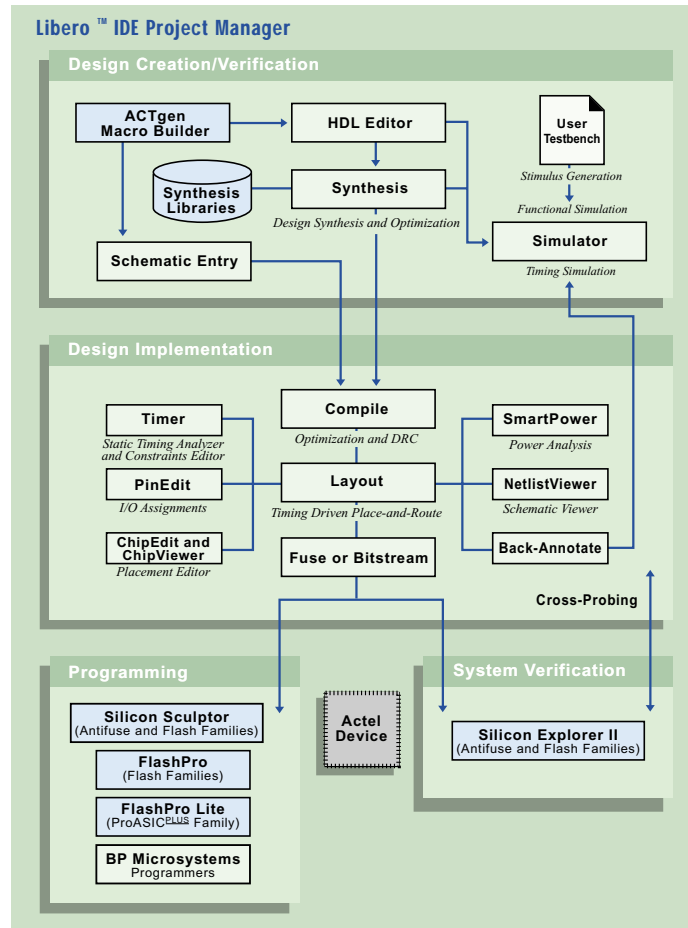


Figure 12 • Design Flow

2.5V/3.3V/5V Operating Conditions

Absolute Maximum Ratings¹

Symbol	Parameter	Limits	Units
V_{CCI}	DC Supply Voltage	-0.3 to +6.0	V
V_{CCA}	DC Supply Voltage	-0.3 to +3.0	V
V_I	Input Voltage	-0.5 to +5.75	V
V_O	Output Voltage	-0.5 to + V_{CCI}	V
T_{STG}	Storage Temperature	-65 to +150	°C

Note:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.

Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range ¹	0 to +70	-40 to +85	-55 to +125	°C
2.5V Power Supply Range	2.25 to 2.75	2.25 to 2.75	2.25 to 2.75	V
3.3V Power Supply Range	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
5V Power Supply Range	4.75 to 5.25	4.75 to 5.25	4.75 to 5.25	V

Note:

1. Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.

3.3V LVTTTL and 5V TTL Electrical Specifications

Symbol	Parameter	Commercial		Industrial		Units
		Min.	Max.	Min.	Max.	
V_{OH}	$V_{CCI} = \text{MIN}$ $V_I = V_{IH}$ or V_{IL}	$(I_{OH} = -1\text{mA})$ 0.9 V_{CCI}		0.9 V_{CCI}		V
	$V_{CCI} = \text{MIN}, V_{CCI}$ $V_I = V_{IH}$ or V_{IL}	$(I_{OH} = -8\text{mA})$ 2.4		2.4		V
V_{OL}	$V_{CCI} = \text{MIN}, V_{CCI}$ $V_I = V_{IH}$ or V_{IL}	$(I_{OL} = 1\text{mA})$ 0.4		0.4		V
	$V_{CCI} = \text{MIN}, V_{CCI}$ $V_I = V_{IH}$ or V_{IL}	$(I_{OL} = 12\text{mA})$ 0.4		0.4		V
V_{IL}	Input Low Voltage	0.8		0.8		V
V_{IH}	Input High Voltage	2.0 $V_{CCI} + 0.5$		2.0 $V_{CCI} + 0.5$		V
I_{IL}/I_{IH}	Input Leakage Current, $V_{IN} = V_{CCI}$ or GND	-10	10	-10	10	μA
I_{OZ}	3-State Output Leakage Current	-10	10	-10	10	μA
t_R, t_F	Input Transition Time t_R, t_F	10		10		ns
C_{IO}	I/O Capacitance	10		10		pF
I_{CC}	Standby Current	10		20		mA
IV Curve*	Can be derived from the IBIS model on the web.					

Note: *The IBIS model can be found at www.actel.com/support/support_ibis.html.

2.5V LVCMOS2 Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V _{OH}	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -100μA)	2.1		2.1		V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -1 mA)	2.0		2.0		V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OH} = -2 mA)	1.7		1.7		V
V _{OL}	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 100μA)		0.2		0.2	V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 1mA)		0.4		0.4	V
	V _{DD} = MIN, V _I = V _{IH} or V _{IL}	(I _{OL} = 2 mA)		0.7		0.7	V
V _{IL}	Input Low Voltage, V _{OUT} ≤ V _{VOL(max)}		-0.3	0.7	-0.3	0.7	V
V _{IH}	Input High Voltage, V _{OUT} ≥ V _{VOH(min)}		1.7	V _{DD} + 0.3	1.7	V _{DD} + 0.3	V
I _{OZ}	3-State Output Leakage Current, V _{OUT} = V _{CCI} or GND		-10	10	-10	10	μA
t _R , t _F	Input Transition Time t _R , t _F			10		10	ns
C _{IO}	I/O Capacitance			10		10	pF
I _{CC}	Standby Current			10		20	mA
IV Curve ¹	Can be derived from the IBIS model on the web.						

Note:

1. The IBIS model can be found at www.actel.com/support/support/support_ibis.html.

PCI Compliance for the SX-A Family

The SX-A family supports 3.3V and 5V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

DC Specifications (5V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.3	2.7	V
V_{CCI}	Supply Voltage for I/Os		4.75	5.25	V
V_{IH}	Input High Voltage		2.0	$V_{CCI} + 0.5$	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
I_{IH}	Input High Leakage Current ¹	$V_{IN} = 2.7$		70	μ A
I_{IL}	Input Low Leakage Current ¹	$V_{IN} = 0.5$		-70	μ A
V_{OH}	Output High Voltage	$I_{OUT} = -2$ mA	2.4		V
V_{OL}	Output Low Voltage ²	$I_{OUT} = 3$ mA, 6 mA		0.55	V
C_{IN}	Input Pin Capacitance ³			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
2. *Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter includes FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*

AC Specifications (5V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 1.4$ ¹	-44		mA
		$1.4 \leq V_{OUT} < 2.4$ ^{1, 2}	$(-44 + (V_{OUT} - 1.4)/0.024)$		mA
		$3.1 < V_{OUT} < V_{CCI}$ ^{1, 3}		Equation A on page 18	
	(Test Point)	$V_{OUT} = 3.1$ ³		-142	mA
$I_{OL(AC)}$	Switching Current Low	$V_{OUT} \geq 2.2$ ¹	95		mA
		$2.2 > V_{OUT} > 0.55$ ¹	$(V_{OUT}/0.023)$		mA
		$0.71 > V_{OUT} > 0$ ^{1, 3}		Equation B on page 18	
	(Test Point)	$V_{OUT} = 0.71$ ³		206	mA
I_{CL}	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	0.4V to 2.4V load ⁴	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4V to 0.4V load ⁴	1	5	V/ns

Notes:

1. Refer to the V/I curves in Figure 13 on page 18. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.
3. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 13 on page 18. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
4. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.

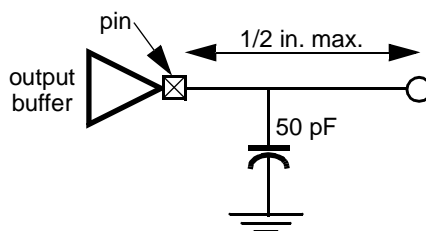


Figure 13 shows the 5V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

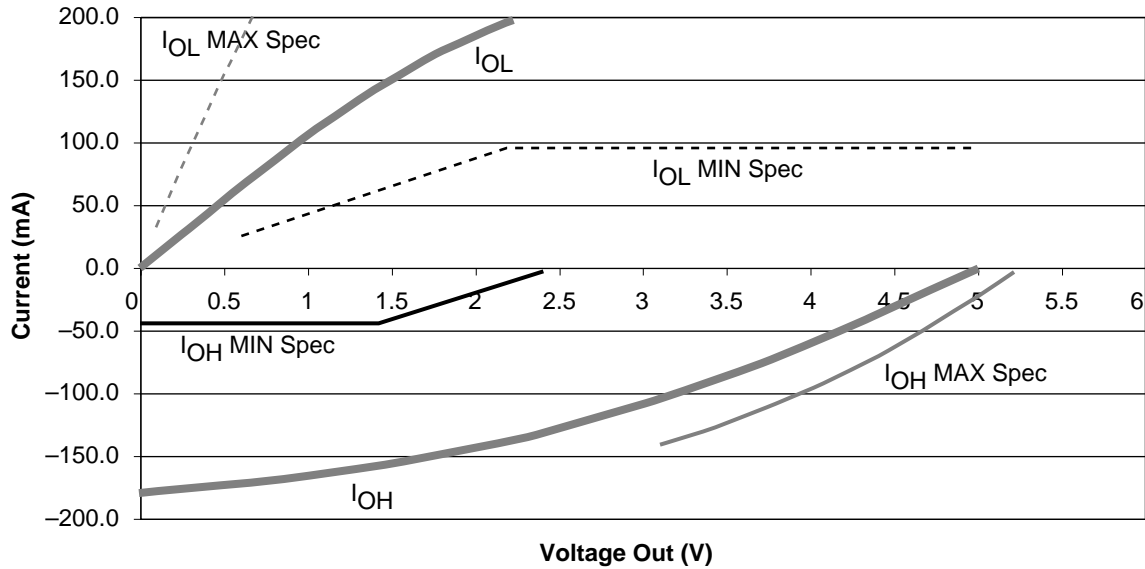


Figure 13 • 5V PCI V/I Curve for SX-A Family

Equation A

$$I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$$

for $V_{CCI} > V_{OUT} > 3.1V$

Equation B

$$I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$$

for $0V < V_{OUT} < 0.71V$

DC Specifications (3.3V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.3	2.7	V
V_{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CCI}$	$V_{CCI} + 0.5$	V
V_{IL}	Input Low Voltage		-0.5	$0.3V_{CCI}$	V
I_{IPU}	Input Pull-up Voltage ¹		$0.7V_{CCI}$		V
I_{IL}	Input Leakage Current ²	$0 < V_{IN} < V_{CCI}$	-10	+10	μA
V_{OH}	Output High Voltage	$I_{OUT} = -500 \mu A$	$0.9V_{CCI}$		V
V_{OL}	Output Low Voltage	$I_{OUT} = 1500 \mu A$		$0.1V_{CCI}$	V
C_{IN}	Input Pin Capacitance ³			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

- This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers should ensure that the input buffer is conducting minimum current at this input voltage in applications sensitive to static power utilization.
- Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
- Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

AC Specifications (3.3V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 0.3V_{CCI}^1$	$-12V_{CCI}$		mA
		$0.3V_{CCI} \leq V_{OUT} < 0.9V_{CCI}^1$	$(-17.1(V_{CCI} - V_{OUT}))$		mA
		$0.7V_{CCI} < V_{OUT} < V_{CCI}^{1,2}$		Equation C on page 20	
	(Test Point)	$V_{OUT} = 0.7V_{CC}^2$		$-32V_{CCI}$	mA
$I_{OL(AC)}$	Switching Current Low	$V_{CCI} > V_{OUT} \geq 0.6V_{CCI}^1$	$16V_{CCI}$		mA
		$0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}^1$	$(26.7V_{OUT})$		mA
		$0.18V_{CCI} > V_{OUT} > 0^{1,2}$		Equation D on page 20	
	(Test Point)	$V_{OUT} = 0.18V_{CC}^2$		$38V_{CCI}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$V_{CCI} + 4 > V_{IN} \geq V_{CCI} + 1$	$25 + (V_{IN} - V_{CCI} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	$0.2V_{CCI} - 0.6V_{CCI}$ load ³	1	4	V/ns
$slew_F$	Output Fall Slew Rate	$0.6V_{CCI} - 0.2V_{CCI}$ load ³	1	4	V/ns

Notes:

1. Refer to the V/I curves in Figure 14 on page 20. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 14 on page 20. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
3. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.

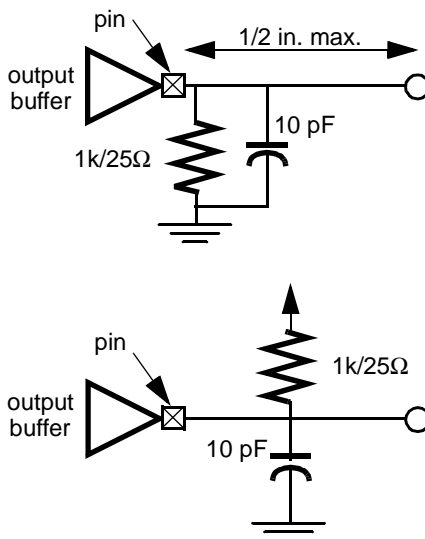


Figure 14 shows the 3.3V PCI V/I curve and the minimum and maximum PCI drive characteristics of the SX-A family.

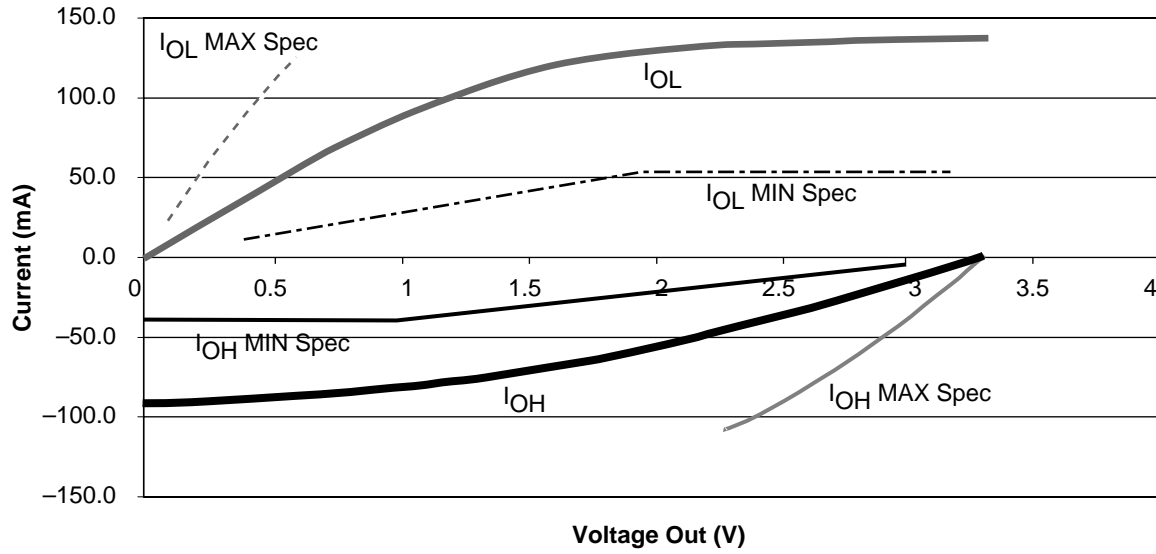


Figure 14 • 3.3V PCI V/I Curve for SX-A Family

Equation C

$$I_{OH} = (98.0/V_{CC1}) * (V_{OUT} - V_{CC1}) * (V_{OUT} + 0.4V_{CC1})$$

for $0.7 V_{CC1} < V_{OUT} < V_{CC1}$

Equation D

$$I_{OL} = (256/V_{CC1}) * V_{OUT} * (V_{CC1} - V_{OUT})$$

for $0V < V_{OUT} < 0.18 V_{CC1}$

Junction Temperature (T_j)

The temperature variable in the Designer Series software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Equation 1, shown below, can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a \quad (1)$$

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient

$$\Delta T = \theta_{ja} * P \quad (2)$$

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (}^\circ\text{C)} - \text{Max. ambient temp. (}^\circ\text{C)}}{\theta_{ja}(\text{}^\circ\text{C/W)}} = \frac{150^\circ\text{C} - 70^\circ\text{C}}{28^\circ\text{C/W}} = 2.86\text{W}$$

P = Power

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the Package Thermal Characteristics table below.

Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc} , and the junction-to-ambient air characteristic is θ_{ja} . The thermal characteristics for θ_{ja} are shown with two different air flow rates.

The maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a TQFP 176-pin package at commercial temperature and still air is as follows:

Package Thermal Characteristics

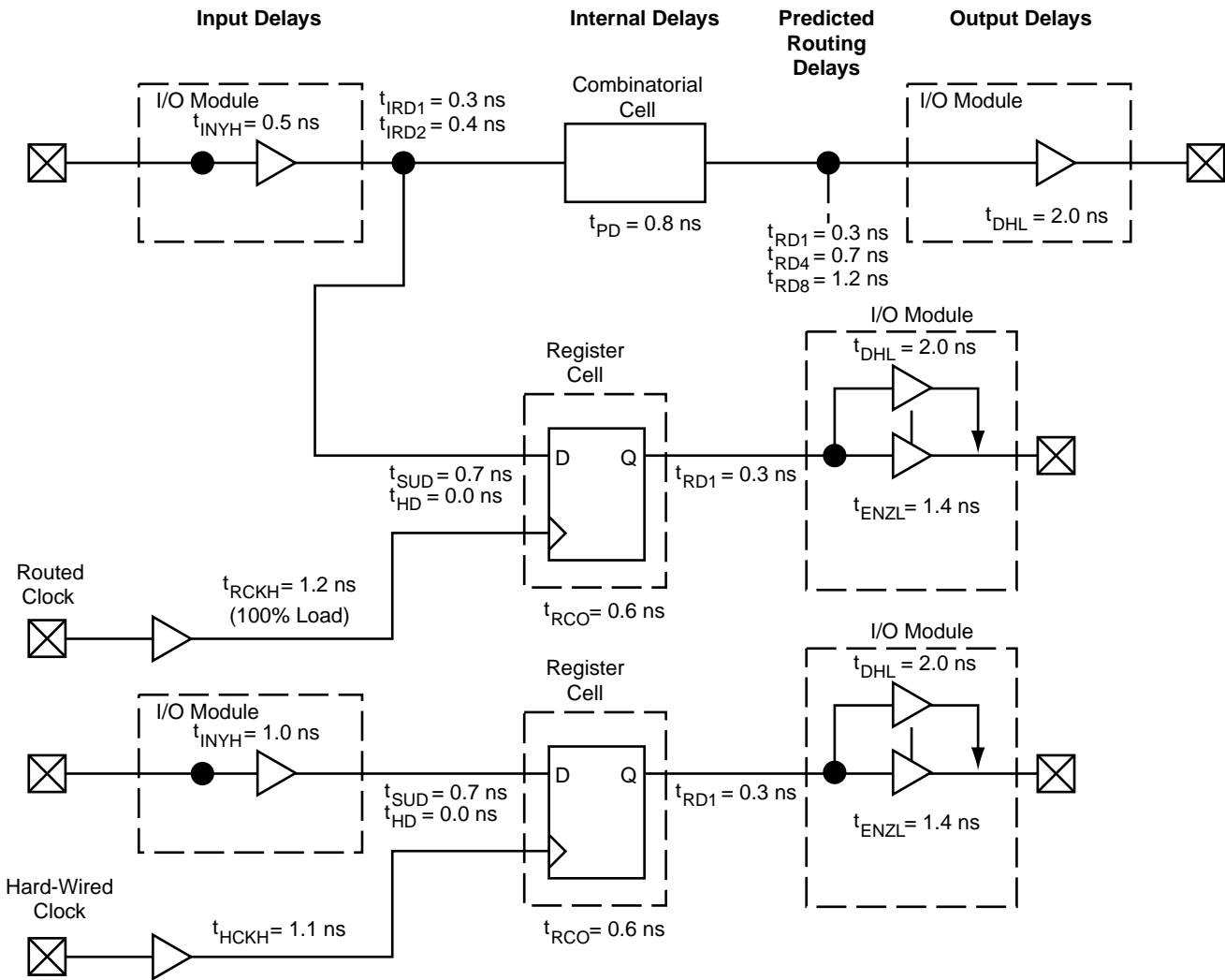
Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min	Units
Thin Quad Flat Pack (TQFP)	100	12	37.5	30	°C/W
Thin Quad Flat Pack (TQFP)	144	11	32	24	°C/W
Thin Quad Flat Pack (TQFP)	176	11	28	21	°C/W
Plastic Quad Flat Pack (PQFP) ¹	208	8	30	23	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader ²	208	3.8	20	17	°C/W
Plastic Ball Grid Array (PBGA)	329	3	18	13.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	38.8	26.7	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.3	30	25	°C/W
Fine Pitch Ball Grid Array (FBGA)	484	3	20	15	°C/W

1. The A54SX08A PQ208 has no heat spreader.

2. The SX-A PQ208 package has a heat spreader for A54SX16A, A54SX32A, and A54SX72A.

For Power Estimator information, please go to <http://www.actel.com/products/tools/index.html>.

SX-A Timing Model*



Note: *Values shown for A54SX08A, -3, worst-case commercial conditions at 3.3V PCI with standard place-and-route.

Sample Path Calculations

Hardwired Clock

$$\begin{aligned} \text{External Setup} &= (t_{INYH} + t_{IRD2} + t_{SUD}) - t_{HCKH} \\ &= 0.5 + 0.4 + 0.7 - 1.1 = 0.5 \text{ ns} \end{aligned}$$

Clock-to-Out (Pad-to-Pad)

$$\begin{aligned} &= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.1 + 0.6 + 0.3 + 2.0 = 4.0 \text{ ns} \end{aligned}$$

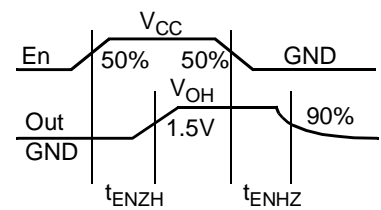
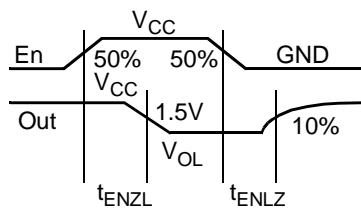
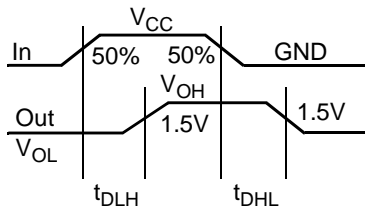
Routed Clock

$$\begin{aligned} \text{External Setup} &= (t_{INYH} + t_{IRD2} + t_{SUD}) - t_{RCKH} \\ &= 0.5 + 0.4 + 0.7 - 1.2 = 0.4 \text{ ns} \end{aligned}$$

Clock-to-Out (Pad-to-Pad)

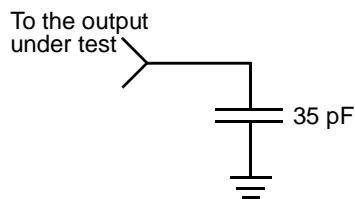
$$\begin{aligned} &= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.2 + 0.6 + 0.3 + 2.0 = 4.1 \text{ ns} \end{aligned}$$

Output Buffer Delays

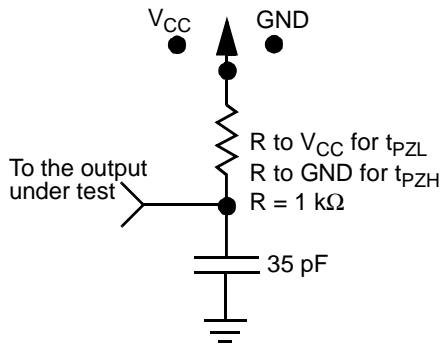


AC Test Loads

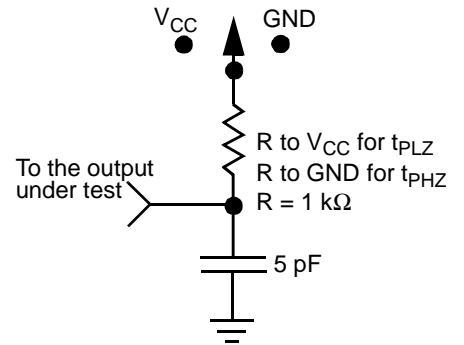
Load 1
(Used to measure propagation delay)



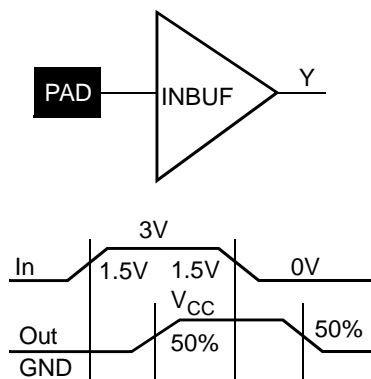
Load 2
(Used to measure enable delays)



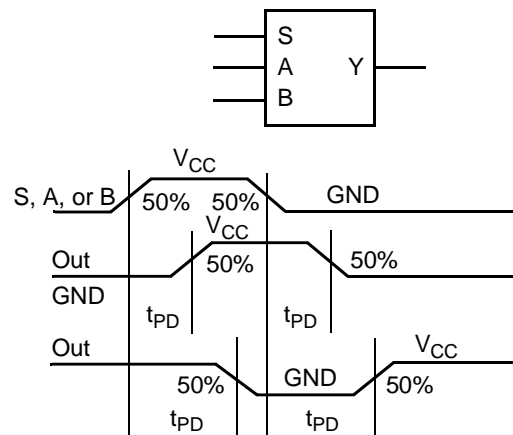
Load 3
(Used to measure disable delays)



Input Buffer Delays

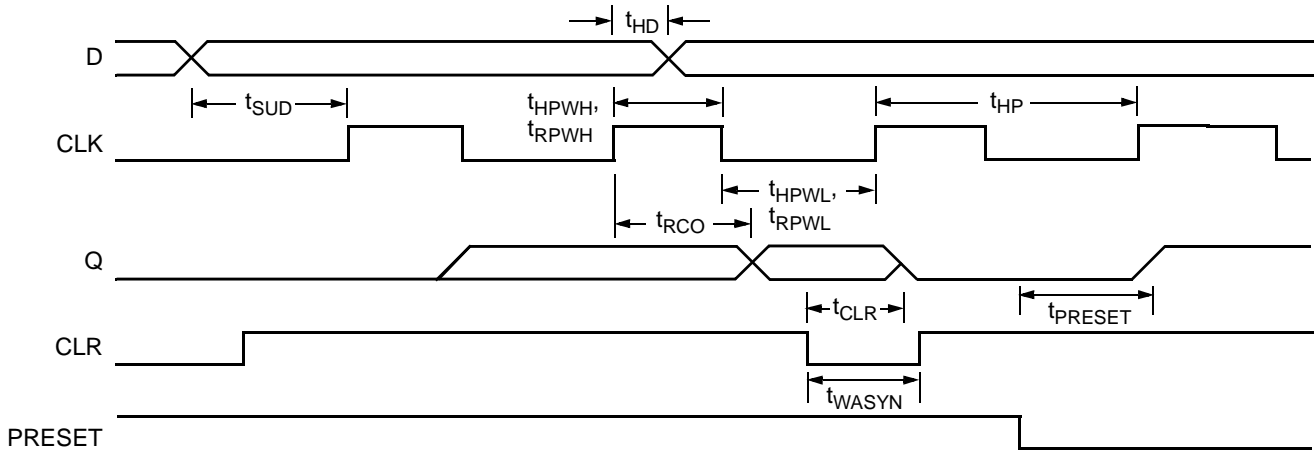
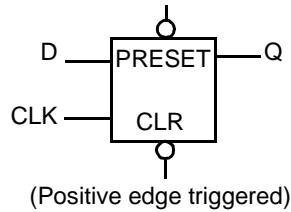


C-Cell Delays



Cell Timing Characteristics

Flip-Flops



Timing Characteristics

Timing characteristics for SX-A devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX-A family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. Delay values may then be determined by using the Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6 percent of the nets in a design may be designated as critical, while 90 percent of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

Timing Derating

SX-A devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

(Normalized to Worst-Case Commercial, $T_J = 70^\circ\text{C}$, $V_{CCA} = 2.3\text{V}$)

V_{CCA}	Junction Temperature (T_J)						
	-55°C	-40°C	0°C	25°C	70°C	85°C	125°C
2.3V	0.75	0.79	0.88	0.89	1.00	1.04	1.16
2.5V	0.70	0.74	0.82	0.83	0.93	0.97	1.08
2.7V	0.66	0.69	0.79	0.79	0.88	0.92	1.02

A54SX08A Timing Characteristics

(Worst-Case Commercial Conditions, $V_{CCA} = 2.3V$, $V_{CCI} = 3.0V$, $T_J = 70^\circ C$)

		'-3' Speed	'-2' Speed	'-1' Speed	'Std' Speed	'-F' Speed	
Parameter	Description	Min. Max.	Min. Max.	Min. Max.	Min. Max.	Min. Max.	Units
C-Cell Propagation Delays¹							
t_{PD}	Internal Array Module	0.8	1.0	1.1	1.3	1.8	ns
Predicted Routing Delays²							
t_{DC}	FO=1 Routing Delay, Direct Connect	0.1	0.1	0.1	0.1	0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect	0.3	0.3	0.3	0.4	0.6	ns
t_{RD1}	FO=1 Routing Delay	0.3	0.3	0.4	0.5	0.6	ns
t_{RD2}	FO=2 Routing Delay	0.4	0.5	0.5	0.6	0.8	ns
t_{RD3}	FO=3 Routing Delay	0.5	0.6	0.7	0.8	1.1	ns
t_{RD4}	FO=4 Routing Delay	0.7	0.8	0.9	1.0	1.4	ns
t_{RD8}	FO=8 Routing Delay	1.2	1.4	1.5	1.8	2.5	ns
t_{RD12}	FO=12 Routing Delay	1.7	2.0	2.2	2.6	3.6	ns
R-Cell Timing							
t_{RCO}	Sequential Clock-to-Q	0.6	0.7	0.8	0.9	1.3	ns
t_{CLR}	Asynchronous Clear-to-Q	0.7	0.8	0.9	1.1	1.6	ns
t_{PRESET}	Asynchronous Preset-to-Q	0.7	0.8	0.9	1.1	1.6	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.7	0.8	0.9	1.1	1.6	ns
t_{HD}	Flip-Flop Data Input Hold	0.0	0.0	0.0	0.0	0.0	ns
t_{WASYN}	Asynchronous Pulse Width	1.3	1.5	1.7	2.0	2.8	ns
$t_{RECA SYN}$	Asynchronous Recovery Time	0.3	0.4	0.4	0.5	0.7	ns
t_{HASYN}	Asynchronous Hold Time	0.3	0.3	0.3	0.4	0.6	ns
Input Module Propagation Delays							
t_{INYH}	Input Data Pad-to-Y HIGH	0.5	0.6	0.7	0.8	1.1	ns
t_{INYL}	Input Data Pad-to-Y LOW	0.8	1.0	1.0	1.3	1.8	ns
Input Module Predicted Routing Delays²							
t_{IRD1}	FO=1 Routing Delay	0.3	0.3	0.3	0.4	0.6	ns
t_{IRD2}	FO=2 Routing Delay	0.4	0.5	0.5	0.6	0.8	ns
t_{IRD3}	FO=3 Routing Delay	0.5	0.6	0.7	0.8	1.1	ns
t_{IRD4}	FO=4 Routing Delay	0.7	0.8	0.9	1.0	1.4	ns
t_{IRD8}	FO=8 Routing Delay	1.2	1.4	1.5	1.8	2.5	ns
t_{IRD12}	FO=12 Routing Delay	1.7	2.0	2.2	2.6	3.6	ns

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

A54SX08A Timing Characteristics (Continued)

 (Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CC1} = 2.3V$, $T_J = 70^\circ C$)

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.1		1.3		1.5		1.8		2.4	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.2		1.4		1.6		2.2	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{HCKSW}	Maximum Skew		0.2		0.2		0.2		0.3		0.4	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.2		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		238		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.1		1.2		1.3		1.6		2.2	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		1.3		1.4		1.6		1.9		2.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		1.2		1.4		1.6		1.9		2.6	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		1.4		1.6		1.9		2.2		3.0	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		1.3		1.5		1.7		2.0		2.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		1.5		1.7		2.0		2.3		3.1	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.3		0.3		0.3		0.3		0.4	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.3		0.3		0.4		0.4		0.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.3		0.3		0.4		0.4		0.7	ns

A54SX08A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 3.0V$, $T_J = 70^{\circ}C$)

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.1		1.2		1.4		1.6		2.4	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.0		1.2		1.3		1.5		2.3	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{HCKSW}	Maximum Skew		0.2		0.2		0.2		0.3		0.4	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.2		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		238		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.0		1.2		1.3		1.6		2.2	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		1.3		1.4		1.7		2.0		2.8	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		1.1		1.3		1.5		1.8		2.5	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		1.4		1.5		1.9		2.2		3.1	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		1.2		1.4		1.6		1.9		2.6	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		1.5		1.6		2.0		2.3		3.4	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.4		0.4	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.3		0.3		0.4		0.4		0.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.3		0.3		0.4		0.4		0.7	ns

A54SX08A Timing Characteristics (Continued)

 (Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CC1} = 4.75V$, $T_J = 70^{\circ}C$)

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.0		1.2		1.4		1.5		2.3	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.0		1.1		1.3		1.5		2.2	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{HCKSW}	Maximum Skew		0.2		0.2		0.2		0.3		0.4	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.2		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		238		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.0		1.1		1.2		1.5		2.0	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		1.2		1.4		1.6		1.8		2.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		1.1		1.3		1.5		1.8		2.5	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		1.3		1.6		1.9		2.1		3.1	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		1.2		1.4		1.6		1.9		2.6	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		1.4		1.7		2.0		2.2		3.2	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.2		0.3		0.3		0.4		0.4	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.3		0.3		0.4		0.4		0.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.3		0.3		0.4		0.4		0.7	ns

A54SX08A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 2.3V$, $T_J = 70^{\circ}C$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2.5V LVTTTL Output Module Timing¹												
t _{DLH}	Data-to-Pad LOW to HIGH		3.2		3.8		4.3		5.0		7.0	ns
t _{DHL}	Data-to-Pad HIGH to LOW		2.6		3.0		3.4		4.0		5.5	ns
t _{DHLS}	Data-to-Pad HIGH to LOW—low slew		11.3		13.0		14.8		17.4		24.4	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.4		2.8		3.2		3.7		5.2	ns
t _{ENZLS}	Data-to-Pad, Z to L—low slew		11.8		13.7		15.5		18.2		25.5	ns
t _{ENZH}	Enable-to-Pad, Z to H		3.4		4.0		4.5		5.3		7.5	ns
t _{ENLZ}	Enable-to-Pad, L to Z		2.1		2.5		2.8		3.3		4.7	ns
t _{ENHZ}	Enable-to-Pad, H to Z		3.4		4.0		4.5		5.3		7.5	ns
d _{TLH}	Delta LOW to HIGH		0.031		0.037		0.043		0.051		0.071	ns/pF
d _{THL}	Delta HIGH to LOW		0.017		0.017		0.023		0.023		0.037	ns/pF
d _{THLS}	Delta HIGH to LOW—low slew		0.057		0.060		0.071		0.086		0.117	ns/pF

Note:

1. Delays based on 35 pF loading.

A54SX08A Timing Characteristics (Continued)

 (Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 3.0V$, $T_J = 70^\circ C$)

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		
Parameter Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
3.3V PCI Output Module Timing¹												
t_{DLH}	Data-to-Pad LOW to HIGH	2.0		2.3		2.6		3.0		4.3		ns
t_{DHL}	Data-to-Pad HIGH to LOW	2.0		2.3		2.6		3.0		4.3		ns
t_{ENZL}	Enable-to-Pad, Z to L	1.4		1.7		1.9		2.2		3.1		ns
t_{ENZH}	Enable-to-Pad, Z to H	1.4		1.7		1.9		2.2		3.1		ns
t_{ENLZ}	Enable-to-Pad, L to Z	2.5		2.8		3.2		3.8		5.3		ns
t_{ENHZ}	Enable-to-Pad, H to Z	2.5		2.8		3.2		3.8		5.3		ns
d_{TLH}	Delta LOW to HIGH	0.025		0.03		0.03		0.04		0.045		ns/pF
d_{THL}	Delta HIGH to LOW	0.015		0.015		0.015		0.015		0.025		ns/pF
3.3V LVTTTL Output Module Timing²												
t_{DLH}	Data-to-Pad LOW to HIGH	2.7		3.2		3.6		4.2		5.9		ns
t_{DHL}	Data-to-Pad HIGH to LOW	2.5		2.8		3.2		3.8		5.3		ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew	9.0		10.4		11.8		13.8		19.4		ns
t_{ENZL}	Enable-to-Pad, Z to L	2.2		2.6		2.9		3.4		4.8		ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew	15.8		18.9		21.3		25.4		34.9		ns
t_{ENZH}	Enable-to-Pad, Z to H	2.9		3.3		3.7		4.4		6.2		ns
t_{ENLZ}	Enable-to-Pad, L to Z	2.9		3.3		3.7		4.4		6.2		ns
t_{ENHZ}	Enable-to-Pad, H to Z	2.5		2.8		3.2		3.8		5.3		ns
d_{TLH}	Delta LOW to HIGH	0.025		0.03		0.03		0.04		0.045		ns/pF
d_{THL}	Delta HIGH to LOW	0.015		0.015		0.015		0.015		0.025		ns/pF
d_{THLS}	Delta HIGH to LOW—low slew	0.053		0.053		0.067		0.073		0.107		ns/pF

Notes:

1. Delays based on 10 pF loading and 25 Ω resistance.
2. Delays based on 35 pF loading.

A54SX08A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 4.75V$, $T_J = 70^\circ C$)

Parameter Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5.0V PCI Output Module Timing¹											
t _{DLH}	Data-to-Pad LOW to HIGH		2.1	2.5	2.8	3.3	4.6	ns			
t _{DHL}	Data-to-Pad HIGH to LOW		2.7	3.1	3.5	4.2	5.8	ns			
t _{DHLS}	Data-to-Pad HIGH to LOW—low slew		7.4	8.5	9.6	11.3	15.9	ns			
t _{ENZL}	Enable-to-Pad, Z to L		1.3	1.5	1.7	2.0	2.8	ns			
t _{ENZLS}	Enable-to-Pad, Z to L—low slew		3.5	5.1	5.9	6.9	9.7	ns			
t _{ENZH}	Enable-to-Pad, Z to H		1.3	1.5	1.7	2.0	2.8	ns			
t _{ENLZ}	Enable-to-Pad, L to Z		3.0	3.5	3.9	4.6	6.4	ns			
t _{ENHZ}	Enable-to-Pad, H to Z		3.0	3.5	3.9	4.6	6.4	ns			
d _{TLH}	Delta LOW to HIGH		0.016	0.016	0.02	0.022	0.032	ns/pF			
d _{THL}	Delta HIGH to LOW		0.026	0.03	0.032	0.04	0.052	ns/pF			
d _{THLS}	Delta HIGH to LOW—low slew		0.04	0.052	0.06	0.07	0.096	ns/pF			
5.0V TTL Output Module Timing²											
t _{DLH}	Data-to-Pad LOW to HIGH		1.9	2.2	2.5	3.0	4.2	ns			
t _{DHL}	Data-to-Pad HIGH to LOW		2.5	2.9	3.3	3.9	5.4	ns			
t _{DHLS}	Data-to-Pad HIGH to LOW—low slew		6.6	7.6	8.6	10.2	14.2	ns			
t _{ENZL}	Enable-to-Pad, Z to L		2.1	2.4	2.7	3.2	4.5	ns			
t _{ENZLS}	Enable-to-Pad, Z to L—low slew		7.4	8.4	9.5	11.0	15.4	ns			
t _{ENZH}	Enable-to-Pad, Z to H		2.3	2.7	3.1	3.6	5.0	ns			
t _{ENLZ}	Enable-to-Pad, L to Z		3.6	4.2	4.7	5.6	7.8	ns			
t _{ENHZ}	Enable-to-Pad, H to Z		3.0	3.5	3.9	4.6	6.4	ns			
d _{TLH}	Delta LOW to HIGH		0.014	0.017	0.017	0.023	0.031	ns/pF			
d _{THL}	Delta HIGH to LOW		0.023	0.029	0.031	0.037	0.051	ns/pF			
d _{THLS}	Delta HIGH to LOW—low slew		0.043	0.046	0.057	0.066	0.089	ns/pF			

Notes:

1. Delays based on 50 pF loading.
2. Delays based on 35 pF loading.

A54SX16A Timing Characteristics

(Worst-Case Commercial Conditions, $V_{CCA} = 2.3V$, $V_{CCI} = 3.0V$, $T_J = 70^\circ C$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays¹												
t_{PD}	Internal Array Module	0.8		1.0		1.1		1.3		1.8		ns
Predicted Routing Delays²												
t_{DC}	FO=1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		0.1		ns
t_{FC}	FO=1 Routing Delay, Fast Connect	0.3		0.3		0.3		0.4		0.6		ns
t_{RD1}	FO=1 Routing Delay	0.3		0.3		0.4		0.5		0.6		ns
t_{RD2}	FO=2 Routing Delay	0.4		0.5		0.5		0.6		0.8		ns
t_{RD3}	FO=3 Routing Delay	0.5		0.6		0.7		0.8		1.1		ns
t_{RD4}	FO=4 Routing Delay	0.7		0.8		0.9		1.0		1.4		ns
t_{RD8}	FO=8 Routing Delay	1.2		1.4		1.5		1.8		2.5		ns
t_{RD12}	FO=12 Routing Delay	1.7		2.0		2.2		2.6		3.6		ns
R-Cell Timing												
t_{RCO}	Sequential Clock-to-Q	0.6		0.7		0.8		0.9		1.3		ns
t_{CLR}	Asynchronous Clear-to-Q	0.7		0.8		0.9		1.1		1.6		ns
t_{PRESET}	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.1		1.6		ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.1		1.6		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.3		1.5		1.7		2.0		2.8		ns
t_{REASYN}	Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t_{HASYN}	Asynchronous Removal Time	0.3		0.3		0.3		0.4		0.6		ns
Input Module Propagation Delays												
t_{INYH}	Input Data Pad-to-Y HIGH	0.5		0.6		0.7		0.8		1.1		ns
t_{INYL}	Input Data Pad-to-Y LOW	0.8		1.0		1.0		1.3		1.8		ns
Input Module Predicted Routing Delays²												
t_{IRD1}	FO=1 Routing Delay	0.3		0.3		0.3		0.4		0.6		ns
t_{IRD2}	FO=2 Routing Delay	0.4		0.5		0.5		0.6		0.8		ns
t_{IRD3}	FO=3 Routing Delay	0.5		0.6		0.7		0.8		1.1		ns
t_{IRD4}	FO=4 Routing Delay	0.7		0.8		0.9		1.0		1.4		ns
t_{IRD8}	FO=8 Routing Delay	1.2		1.4		1.5		0.8		2.5		ns
t_{IRD12}	FO=12 Routing Delay	1.7		2.0		2.2		2.6		3.6		ns

Notes:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

A54SX16A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 2.3V$, $T_J = 70^\circ C$)

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.2		1.5		1.6		1.9		2.9	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.4		1.5		1.8		2.8	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{HCKSW}	Maximum Skew		0.1		0.1		0.1		0.1		0.2	ns
t_{HP}	Minimum Period	2.7		3.2		3.6		4.2		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		238		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.2		1.3		1.5		1.8		2.5	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		1.3		1.4		1.6		1.9		2.7	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		1.5		1.7		2.0		2.3		3.3	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		1.6		1.8		2.1		2.4		3.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		1.7		1.9		2.2		2.6		3.6	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		1.8		2.0		2.3		2.7		3.8	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.3		0.4		0.4		0.4		0.6	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.5		0.6		0.7		0.8		1.3	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.5		0.6		0.7		0.8		1.3	ns

A54SX16A Timing Characteristics (Continued)

 (Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 3.0V$, $T_J = 70^\circ C$)

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.2		1.5		1.6		1.9		2.9	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.4		1.5		1.8		2.8	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{HCKSW}	Maximum Skew		0.1		0.1		0.1		0.1		0.2	ns
t_{HP}	Minimum Period	2.7		3.2		3.6		4.2		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		238		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.2		1.3		1.5		1.8		2.4	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		1.3		1.4		1.7		2.0		2.8	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		1.5		1.7		2.0		2.3		3.3	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		1.6		1.8		2.1		2.4		3.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		1.7		1.9		2.2		2.6		3.6	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		1.8		2.0		2.3		2.7		3.8	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.3		0.4		0.4		0.4		0.6	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.5		0.6		0.7		0.8		1.3	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.5		0.6		0.7		0.8		1.3	ns

A54SX16A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 4.75V$, $T_J = 70^\circ C$)

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.2		1.4		1.6		1.8		2.8	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.3		1.5		1.7		2.7	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{HCKSW}	Maximum Skew		0.1		0.1		0.1		0.1		0.2	ns
t_{HP}	Minimum Period	2.7		3.2		3.6		4.2		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		238		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.1		1.2		1.4		1.7		2.3	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		1.2		1.4		1.6		1.8		2.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		1.4		1.6		1.8		2.2		3.1	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		1.5		1.7		1.9		2.3		3.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		1.6		1.9		2.1		2.5		3.5	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		1.7		2.0		2.2		2.6		4.0	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.1		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.1		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.3		0.4		0.4		0.4		0.6	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.5		0.6		0.7		0.8		1.3	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.5		0.6		0.7		0.8		1.3	ns

A54SX16A Timing Characteristics (Continued)

 (Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 2.3V$, $T_J = 70^\circ C$)

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		
Parameter Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
2.5V LVTTTL Output Module Timing¹												
t_{DLH}	Data-to-Pad LOW to HIGH		3.2		3.8		4.3		5.0		7.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.6		3.0		3.4		4.0		5.5	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		11.3		13.0		14.8		17.4		24.4	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.4		2.8		3.2		3.7		5.2	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		11.8		13.7		15.5		18.2		25.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.4		4.0		4.5		5.3		7.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		2.5		2.8		3.3		4.7	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.4		4.0		4.5		5.3		7.5	ns
d_{TLH}	Delta LOW to HIGH		0.031		0.037		0.043		0.051		0.071	ns/pF
d_{THL}	Delta HIGH to LOW		0.017		0.017		0.023		0.023		0.037	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.057		0.060		0.071		0.086		0.117	ns/pF

Note:

1. Delays based on 35 pF loading.

A54SX16A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 3.0V$, $T_J = 70^\circ C$)

Parameter Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3V PCI Output Module Timing¹											
t _{DLH} Data-to-Pad LOW to HIGH		2.0		2.3		2.6		3.0		4.3	ns
t _{DHL} Data-to-Pad HIGH to LOW		2.0		2.3		2.6		3.0		4.3	ns
t _{ENZL} Enable-to-Pad, Z to L		1.4		1.7		1.9		2.2		3.1	ns
t _{ENZH} Enable-to-Pad, Z to H		1.4		1.7		1.9		2.2		3.1	ns
t _{ENLZ} Enable-to-Pad, L to Z		2.5		2.8		3.2		3.8		5.3	ns
t _{ENHZ} Enable-to-Pad, H to Z		2.5		2.8		3.2		3.8		5.3	ns
d _{TLH} Delta LOW to HIGH		0.025		0.03		0.03		0.04		0.045	ns/pF
d _{THL} Delta HIGH to LOW		0.015		0.015		0.015		0.015		0.025	ns/pF
3.3V LVTTTL Output Module Timing²											
t _{DLH} Data-to-Pad LOW to HIGH		2.7		3.2		3.6		4.2		5.9	ns
t _{DHL} Data-to-Pad HIGH to LOW		2.5		2.8		3.2		3.8		5.3	ns
t _{DHLS} Data-to-Pad HIGH to LOW—low slew		9.0		10.4		11.8		13.8		19.4	ns
t _{ENZL} Enable-to-Pad, Z to L		2.2		2.6		2.9		3.4		4.8	ns
t _{ENZLS} Enable-to-Pad, Z to L—low slew		15.8		18.9		21.3		25.4		34.9	ns
t _{ENZH} Enable-to-Pad, Z to H		2.9		3.3		3.7		4.4		6.2	ns
t _{ENLZ} Enable-to-Pad, L to Z		2.9		3.3		3.7		4.4		6.2	ns
t _{ENHZ} Enable-to-Pad, H to Z		2.5		2.8		3.2		3.8		5.3	ns
d _{TLH} Delta LOW to HIGH		0.025		0.03		0.03		0.04		0.045	ns/pF
d _{THL} Delta HIGH to LOW		0.015		0.015		0.015		0.015		0.025	ns/pF
d _{THLS} Delta HIGH to LOW—low slew		0.053		0.053		0.067		0.073		0.107	ns/pF

Notes:

1. Delays based on 10 pF loading and 2 Ω resistance.
2. Delays based on 35 pF loading.

A54SX16A Timing Characteristics (Continued)

 (Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 4.75V$, $T_J = 70^\circ C$)

		‘-3’ Speed		‘-2’ Speed		‘-1’ Speed		‘Std’ Speed		‘-F’ Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
5.0V PCI Output Module Timing¹												
t _{DLH}	Data-to-Pad LOW to HIGH	2.1	2.5	2.8	3.3	4.6	ns					
t _{DHL}	Data-to-Pad HIGH to LOW	2.73	3.1	3.5	4.2	5.8	ns					
t _{DHLS}	Data-to-Pad HIGH to LOW—low slew	7.4	8.5	9.6	11.3	15.9	ns					
t _{ENZL}	Enable-to-Pad, Z to L	1.3	1.5	1.7	2.0	2.8	ns					
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	3.5	5.1	5.9	6.9	9.7	ns					
t _{ENZH}	Enable-to-Pad, Z to H	1.3	1.5	1.7	2.0	2.8	ns					
t _{ENLZ}	Enable-to-Pad, L to Z	3.0	3.5	3.9	4.6	6.4	ns					
t _{ENHZ}	Enable-to-Pad, H to Z	3.0	3.5	3.9	4.6	6.4	ns					
d _{TLH}	Delta LOW to HIGH	0.016	0.016	0.02	0.022	0.032	ns/pF					
d _{THL}	Delta HIGH to LOW	0.026	0.03	0.032	0.04	0.052	ns/pF					
d _{THLS}	Delta HIGH to LOW—low slew	0.04	0.052	0.06	0.07	0.096	ns/pF					
5.0V TTL Output Module Timing²												
t _{DLH}	Data-to-Pad LOW to HIGH	1.9	2.2	2.5	3.0	4.2	ns					
t _{DHL}	Data-to-Pad HIGH to LOW	2.5	2.9	3.3	3.9	5.4	ns					
t _{DHLS}	Data-to-Pad HIGH to LOW—low slew	6.6	7.6	8.6	10.2	14.2	ns					
t _{ENZL}	Enable-to-Pad, Z to L	2.1	2.4	2.7	3.2	4.5	ns					
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	7.4	8.4	9.5	11.0	15.4	ns					
t _{ENZH}	Enable-to-Pad, Z to H	2.3	2.7	3.1	3.6	5.0	ns					
t _{ENLZ}	Enable-to-Pad, L to Z	3.6	4.2	4.7	5.6	7.8	ns					
t _{ENHZ}	Enable-to-Pad, H to Z	3.0	3.5	3.9	4.6	6.4	ns					
d _{TLH}	Delta LOW to HIGH	0.014	0.017	0.017	0.023	0.031	ns/pF					
d _{THL}	Delta HIGH to LOW	0.023	0.029	0.031	0.037	0.051	ns/pF					
d _{THLS}	Delta HIGH to LOW—low slew	0.043	0.046	0.057	0.066	0.089	ns/pF					

Notes:

1. Delays based on 50 pF loading.
2. Delays based on 35 pF loading.

A54SX32A Timing Characteristics

(Worst-Case Commercial Conditions, $V_{CCA} = 2.3V$, $V_{CCI} = 3.0V$, $T_J = 70^\circ C$)

		'-3' Speed	'-2' Speed	'-1' Speed	'Std' Speed	'-F' Speed	
Parameter	Description	Min. Max.	Min. Max.	Min. Max.	Min. Max.	Min. Max.	Units
C-Cell Propagation Delays¹							
t_{PD}	Internal Array Module	0.8	1.0	1.1	1.3	1.8	ns
Predicted Routing Delays²							
t_{DC}	FO=1 Routing Delay, Direct Connect	0.1	0.1	0.1	0.1	0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect	0.3	0.3	0.3	0.4	0.6	ns
t_{RD1}	FO=1 Routing Delay	0.3	0.3	0.4	0.5	0.6	ns
t_{RD2}	FO=2 Routing Delay	0.4	0.5	0.5	0.6	0.8	ns
t_{RD3}	FO=3 Routing Delay	0.5	0.6	0.7	0.8	1.1	ns
t_{RD4}	FO=4 Routing Delay	0.7	0.8	0.9	1.0	1.4	ns
t_{RD8}	FO=8 Routing Delay	1.2	1.4	1.5	1.8	2.5	ns
t_{RD12}	FO=12 Routing Delay	1.7	2.0	2.2	2.6	3.6	ns
R-Cell Timing							
t_{RCO}	Sequential Clock-to-Q	0.6	0.7	0.8	0.9	1.3	ns
t_{CLR}	Asynchronous Clear-to-Q	0.7	0.8	0.9	1.1	1.6	ns
t_{PRESET}	Asynchronous Preset-to-Q	0.7	0.8	0.9	1.1	1.6	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.7	0.8	0.9	1.1	1.6	ns
t_{HD}	Flip-Flop Data Input Hold	0.0	0.0	0.0	0.0	0.0	ns
t_{WASYN}	Asynchronous Pulse Width	1.3	1.5	1.7	2.0	2.8	ns
t_{REASYN}	Asynchronous Recovery Time	0.3	0.4	0.4	0.5	0.7	ns
t_{HASYN}	Asynchronous Removal Time	0.3	0.3	0.3	0.4	0.6	ns
Input Module Propagation Delays							
t_{INYH}	Input Data Pad-to-Y HIGH	0.5	0.6	0.7	0.8	1.1	ns
t_{INYL}	Input Data Pad-to-Y LOW	0.8	1.0	1.0	1.3	1.8	ns
Input Module Predicted Routing Delays²							
t_{IRD1}	FO=1 Routing Delay	0.3	0.3	0.3	0.4	0.6	ns
t_{IRD2}	FO=2 Routing Delay	0.4	0.5	0.5	0.6	0.8	ns
t_{IRD3}	FO=3 Routing Delay	0.5	0.6	0.7	0.8	1.1	ns
t_{IRD4}	FO=4 Routing Delay	0.7	0.8	0.9	1.0	1.4	ns
t_{IRD8}	FO=8 Routing Delay	1.2	1.4	1.5	1.8	2.5	ns
t_{IRD12}	FO=12 Routing Delay	1.7	2.0	2.2	2.6	3.6	ns

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

A54SX32A Timing Characteristics (Continued)

 (Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CC1} = 2.3V$, $T_J = 70^{\circ}C$)

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.7		2.0		2.3		2.7		4.1	ns
t _{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.5		1.7		1.9		2.3		3.5	ns
t _{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t _{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t _{HCKSW}	Maximum Skew		0.3		0.4		0.4		0.5		0.8	ns
t _{HP}	Minimum Period	2.7		3.2		3.6		4.4		6.0		ns
f _{HMAX}	Maximum Frequency		350		310		277		227		166	MHz
Routed Array Clock Networks												
t _{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.7		2.0		2.2		2.6		3.7	ns
t _{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.1		2.4		2.7		3.2		4.5	ns
t _{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		2.1		2.4		2.8		3.2		4.5	ns
t _{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.3		2.5		2.9		3.4		5.0	ns
t _{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		2.5		2.9		3.2		3.8		6.4	ns
t _{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.5		2.9		3.2		3.8		6.4	ns
t _{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t _{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.9		1.0		1.1		1.3		2.2	ns
t _{RCKSW}	Maximum Skew (50% Load)		1.2		1.4		1.6		1.9		3.2	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.3		1.5		1.7		2.0		3.4	ns

A54SX32A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 3.0V$, $T_J = 70^\circ C$)

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.7		2.0		2.3		2.7		4.1	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.5		1.7		1.9		2.3		3.5	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.3		0.4		0.4		0.5		0.8	ns
t_{HP}	Minimum Period	2.7		3.2		3.6		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		227		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.7		2.0		2.2		2.6		3.7	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.1		2.4		2.8		3.3		4.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		2.1		2.4		2.8		3.2		4.5	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.3		2.5		2.9		3.4		5.0	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		2.5		2.9		3.2		3.8		6.4	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.5		2.9		3.2		3.8		6.4	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.9		1.0		1.1		1.3		2.2	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.2		1.4		1.6		1.9		3.2	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.3		1.5		1.7		2.0		3.4	ns

A54SX32A Timing Characteristics (Continued)

 (Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 4.75V$, $T_J = 70^{\circ}C$)

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks												
t _{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.7		1.9		2.3		2.6		4.0	ns
t _{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.5		1.7		1.9		2.2		3.5	ns
t _{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t _{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t _{HCKSW}	Maximum Skew		0.3		0.4		0.4		0.5		0.8	ns
t _{HP}	Minimum Period	2.7		3.2		3.6		4.4		6.0		ns
f _{HMAX}	Maximum Frequency		350		310		277		227		166	MHz
Routed Array Clock Networks												
t _{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.6		1.9		2.1		2.5		3.5	ns
t _{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.0		2.4		2.7		3.1		4.4	ns
t _{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		2.0		2.4		2.7		3.1		2.5	ns
t _{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.2		2.5		2.8		3.3		5.5	ns
t _{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		2.5		2.9		3.2		3.8		6.4	ns
t _{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.5		2.9		3.2		3.8		6.4	ns
t _{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t _{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.9		1.0		1.1		1.3		2.0	ns
t _{RCKSW}	Maximum Skew (50% Load)		1.2		1.4		1.6		1.9		3.2	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.3		1.5		1.7		2.0		3.4	ns

A54SX32A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 2.3V$, $T_J = 70^\circ C$)

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		
Parameter Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
2.5V LVTTL Output Module Timing¹												
t _{DLH}	Data-to-Pad LOW to HIGH	3.2	3.8	4.3	5.0	7.0	ns					
t _{DHL}	Data-to-Pad HIGH to LOW	2.6	3.0	3.4	4.0	5.5	ns					
t _{DHLS}	Data-to-Pad HIGH to LOW—low slew	11.3	13.0	14.8	17.4	24.4	ns					
t _{ENZL}	Enable-to-Pad, Z to L	2.4	2.8	3.2	3.7	5.2	ns					
t _{ENZLS}	Data-to-Pad, Z to L—low slew	11.8	13.7	15.5	18.2	25.5	ns					
t _{ENZH}	Enable-to-Pad, Z to H	3.4	4.0	4.5	5.3	7.5	ns					
t _{ENLZ}	Enable-to-Pad, L to Z	2.1	2.5	2.8	3.3	4.7	ns					
t _{ENHZ}	Enable-to-Pad, H to Z	3.4	4.0	4.5	5.3	7.5	ns					
d _{TLH}	Delta LOW to HIGH	0.031	0.037	0.043	0.051	0.071	ns/pF					
d _{THL}	Delta HIGH to LOW	0.017	0.017	0.023	0.023	0.037	ns/pF					
d _{THLS}	Delta HIGH to LOW—low slew	0.057	0.060	0.071	0.086	0.117	ns/pF					

Note:

1. Delays based on 35 pF loading.

A54SX32A Timing Characteristics (Continued)

 (Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 3.0V$, $T_J = 70^\circ C$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3V PCI Output Module Timing¹												
t _{DLH}	Data-to-Pad LOW to HIGH	2.0		2.3		2.6		3.0		4.3		ns
t _{DHL}	Data-to-Pad HIGH to LOW	2.0		2.3		2.6		3.0		4.3		ns
t _{ENZL}	Enable-to-Pad, Z to L	1.4		1.7		1.9		2.2		3.1		ns
t _{ENZH}	Enable-to-Pad, Z to H	1.4		1.7		1.9		2.2		3.1		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.5		2.8		3.2		3.8		5.3		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.5		2.8		3.2		3.8		5.3		ns
d _{TLH}	Delta LOW to HIGH	0.025		0.03		0.03		0.04		0.045		ns/pF
d _{THL}	Delta HIGH to LOW	0.015		0.015		0.015		0.015		0.025		ns/pF
3.3V LVTTL Output Module Timing²												
t _{DLH}	Data-to-Pad LOW to HIGH	2.7		3.2		3.6		4.2		5.9		ns
t _{DHL}	Data-to-Pad HIGH to LOW	2.5		2.8		3.2		3.8		5.3		ns
t _{DHLS}	Data-to-Pad HIGH to LOW—low slew	9.0		10.4		11.8		13.8		19.4		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.2		2.6		2.9		3.4		4.8		ns
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	15.8		18.9		21.3		25.4		34.9		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.9		3.3		3.7		4.4		6.2		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.9		3.3		3.7		4.4		6.2		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.5		2.8		3.2		3.8		5.3		ns
d _{TLH}	Delta LOW to HIGH	0.025		0.03		0.03		0.04		0.045		ns/pF
d _{THL}	Delta HIGH to LOW	0.015		0.015		0.015		0.015		0.025		ns/pF
d _{THLS}	Delta HIGH to LOW—low slew	0.053		0.053		0.067		0.073		0.107		ns/pF

Notes:

1. Delays based on 10 pF loading and 25Ω resistance.
2. Delays based on 35 pF loading.

A54SX32A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 4.75V$, $T_J = 70^\circ C$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5.0V PCI Output Module Timing¹												
t _{DLH}	Data-to-Pad LOW to HIGH	2.1	2.5	2.8	3.3	4.6	ns					
t _{DHL}	Data-to-Pad HIGH to LOW	2.7	3.1	3.5	4.2	5.8	ns					
t _{DHLS}	Data-to-Pad HIGH to LOW—low slew	7.4	8.5	9.6	11.3	15.9	ns					
t _{ENZL}	Enable-to-Pad, Z to L	1.3	1.5	1.7	2.0	2.8	ns					
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	3.5	5.1	5.9	6.9	9.7	ns					
t _{ENZH}	Enable-to-Pad, Z to H	1.3	1.5	1.7	2.0	2.8	ns					
t _{ENLZ}	Enable-to-Pad, L to Z	3.0	3.5	3.9	4.6	6.4	ns					
t _{ENHZ}	Enable-to-Pad, H to Z	3.0	3.5	3.9	4.6	6.4	ns					
d _{TLH}	Delta LOW to HIGH	0.016	0.016	0.02	0.022	0.032	ns/pF					
d _{THL}	Delta HIGH to LOW	0.026	0.03	0.032	0.04	0.052	ns/pF					
d _{THLS}	Delta HIGH to LOW—low slew	0.04	0.052	0.06	0.07	0.096	ns/pF					
5.0V TTL Output Module Timing²												
t _{DLH}	Data-to-Pad LOW to HIGH	1.9	2.2	2.5	3.0	4.2	ns					
t _{DHL}	Data-to-Pad HIGH to LOW	2.5	2.9	3.3	3.9	5.4	ns					
t _{DHLS}	Data-to-Pad HIGH to LOW—low slew	6.6	7.6	8.6	10.2	14.2	ns					
t _{ENZL}	Enable-to-Pad, Z to L	2.1	2.4	2.7	3.2	4.5	ns					
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	7.4	8.4	9.5	11.0	15.4	ns					
t _{ENZH}	Enable-to-Pad, Z to H	2.3	2.7	3.1	3.6	5.0	ns					
t _{ENLZ}	Enable-to-Pad, L to Z	3.6	4.2	4.7	5.6	7.8	ns					
t _{ENHZ}	Enable-to-Pad, H to Z	3.0	3.5	3.9	4.6	6.4	ns					
d _{TLH}	Delta LOW to HIGH	0.014	0.017	0.017	0.023	0.031	ns/pF					
d _{THL}	Delta HIGH to LOW	0.023	0.029	0.031	0.037	0.051	ns/pF					
d _{THLS}	Delta HIGH to LOW—low slew	0.043	0.046	0.057	0.066	0.089	ns/pF					

Notes:

1. Delays based on 50 pF loading.
2. Delays based on 35 pF loading.

A54SX72A Timing Characteristics

(Worst-Case Commercial Conditions, $V_{CCA} = 2.3V$, $V_{CCI} = 3.0V$, $T_J = 70^{\circ}C$)

Parameter Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays¹											
t_{PD} Internal Array Module	0.8		1.0		1.1		1.3		1.8		ns
Predicted Routing Delays²											
t_{DC} FO=1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		0.1		ns
t_{FC} FO=1 Routing Delay, Fast Connect	0.3		0.3		0.3		0.4		0.6		ns
t_{RD1} FO=1 Routing Delay	0.3		0.3		0.4		0.5		0.7		ns
t_{RD2} FO=2 Routing Delay	0.4		0.5		0.6		0.7		1.0		ns
t_{RD3} FO=3 Routing Delay	0.5		0.7		0.8		0.9		1.3		ns
t_{RD4} FO=4 Routing Delay	0.7		0.9		1.0		1.1		1.5		ns
t_{RD8} FO=8 Routing Delay	1.2		1.5		1.7		2.1		2.9		ns
t_{RD12} FO=12 Routing Delay	1.7		2.2		2.5		3.0		4.2		ns
R-Cell Timing											
t_{RCO} Sequential Clock-to-Q	0.6		0.7		0.8		0.9		1.3		ns
t_{CLR} Asynchronous Clear-to-Q	0.7		0.8		0.9		1.1		1.6		ns
t_{PRESET} Asynchronous Preset-to-Q	0.7		0.8		0.9		1.1		1.6		ns
t_{SUD} Flip-Flop Data Input Set-Up	0.7		0.8		0.9		1.1		1.6		ns
t_{HD} Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WASYN} Asynchronous Pulse Width	1.3		1.5		1.7		2.0		2.8		ns
$t_{RECA SYN}$ Asynchronous Recovery Time	0.3		0.4		0.4		0.5		0.7		ns
t_{HASYN} Asynchronous Hold Time	0.3		0.3		0.3		0.4		0.6		ns
Input Module Propagation Delays											
t_{INYH} Input Data Pad-to-Y HIGH	0.5		0.6		0.7		0.8		1.1		ns
t_{INYL} Input Data Pad-to-Y LOW	0.8		1.0		1.0		1.3		1.8		ns
Input Module Predicted Routing Delays²											
t_{IRD1} FO=1 Routing Delay	0.3		0.3		0.4		0.5		0.7		ns
t_{IRD2} FO=2 Routing Delay	0.4		0.5		0.6		0.7		1.0		ns
t_{IRD3} FO=3 Routing Delay	0.5		0.7		0.8		0.9		1.3		ns
t_{IRD4} FO=4 Routing Delay	0.7		0.9		1.0		1.1		1.5		ns
t_{IRD8} FO=8 Routing Delay	1.2		1.5		1.7		2.1		2.9		ns
t_{IRD12} FO=12 Routing Delay	1.7		2.2		2.5		3.0		4.2		ns

Notes:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

A54SX72A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 2.3V$, $T_J = 70^\circ C$)

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		
Parameter Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.3		1.5		1.7		2.1		3.1	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.3		1.5		1.9		2.9	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.7		0.8		0.9		1.0		1.6	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		227		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		2.3		2.6		2.9		3.5		4.8	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.6		3.1		3.4		4.0		5.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		3.0		3.5		3.9		4.6		6.5	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		3.3		3.8		4.2		4.9		7.1	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		3.7		4.3		4.8		5.7		8.0	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		4.0		4.6		5.1		6.0		8.6	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.8		2.1		2.4		2.7		3.8	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.2		1.4		1.6		1.9		3.2	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.4		1.5		1.7		2.0		3.4	ns

A54SX72A Timing Characteristics (Continued)

 (Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 3.0V$, $T_J = 70^\circ C$)

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		
Parameter Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.3		1.5		1.7		2.1		3.1	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.3		1.5		1.9		2.9	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.7		0.8		0.9		1.0		1.6	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		227		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		2.2		2.6		2.9		3.5		4.8	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.7		3.1		3.5		4.1		5.7	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		3.0		3.5		3.9		4.6		6.5	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		3.3		3.8		4.2		4.9		7.1	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		3.7		4.3		4.8		5.7		8.0	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		4.0		4.6		5.1		6.0		8.6	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.8		2.1		2.4		2.7		3.8	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.2		1.4		1.6		1.9		3.2	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.4		1.5		1.7		2.0		3.4	ns

A54SX72A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 4.75V$, $T_J = 70^\circ C$)

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		
Parameter Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
Dedicated (Hardwired) Array Clock Networks												
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.3		1.4		1.7		2.0		3.0	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.1		1.2		1.5		1.8		2.8	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{HCKSW}	Maximum Skew		0.7		0.8		0.9		1.0		1.6	ns
t_{HP}	Minimum Period	2.8		3.2		3.6		4.4		6.0		ns
f_{HMAX}	Maximum Frequency		350		310		277		227		166	MHz
Routed Array Clock Networks												
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		2.2		2.5		2.8		3.4		4.6	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.6		3.0		3.4		3.9		5.5	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		3.0		3.5		3.9		4.6		6.5	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		3.3		3.8		4.2		4.9		7.1	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		3.7		4.3		4.8		5.7		8.0	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		4.0		4.6		5.1		6.0		8.6	ns
t_{RPWH}	Min. Pulse Width HIGH	1.4		1.6		1.8		2.2		3.0		ns
t_{RPWL}	Min. Pulse Width LOW	1.4		1.6		1.8		2.2		3.0		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.8		2.1		2.4		2.7		3.8	ns
t_{RCKSW}	Maximum Skew (50% Load)				1.4		1.6		1.9		3.2	ns
t_{RCKSW}	Maximum Skew (100% Load)				1.5		1.7		2.0		3.4	ns

A54SX72A Timing Characteristics (Continued)

 (Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 2.3V$, $T_J = 70^\circ C$)

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		
Parameter Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
2.5V LVTTTL Output Module Timing¹												
t_{DLH}	Data-to-Pad LOW to HIGH		3.3		3.9		4.4		5.2		7.2	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.6		3.0		3.4		4.0		5.5	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		11.7		13.5		15.3		18.0		25.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.4		2.8		3.2		3.7		5.2	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		11.8		13.7		15.5		18.2		25.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.4		4.0		4.5		5.3		7.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.1		2.5		2.8		3.3		4.7	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.4		4.0		4.5		5.3		7.5	ns
d_{TLH}	Delta LOW to HIGH		0.031		0.037		0.043		0.051		0.071	ns/pF
d_{THL}	Delta HIGH to LOW		0.017		0.017		0.023		0.023		0.037	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.057		0.060		0.071		0.086		0.117	ns/pF

Note:

1. Delays based on 35 pF loading.

A54SX72A Timing Characteristics (Continued)

(Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 3.0V$, $T_J = 70^\circ C$)

Parameter Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3.3V PCI Output Module Timing¹											
t _{DLH} Data-to-Pad LOW to HIGH	2.0		2.3		2.6		3.0		4.3		ns
t _{DHL} Data-to-Pad HIGH to LOW	2.0		2.3		2.6		3.0		4.3		ns
t _{ENZL} Enable-to-Pad, Z to L	1.4		1.7		1.9		2.2		3.1		ns
t _{ENZH} Enable-to-Pad, Z to H	1.4		1.7		1.9		2.2		3.1		ns
t _{ENLZ} Enable-to-Pad, L to Z	2.5		2.8		3.2		3.8		5.3		ns
t _{ENHZ} Enable-to-Pad, H to Z	2.5		2.8		3.2		3.8		5.3		ns
d _{TLH} Delta LOW to HIGH	0.025		0.03		0.03		0.04		0.045		ns/pF
d _{THL} Delta HIGH to LOW	0.015		0.015		0.015		0.015		0.025		ns/pF
3.3V LVTTTL Output Module Timing²											
t _{DLH} Data-to-Pad LOW to HIGH	2.7		3.2		3.6		4.2		5.9		ns
t _{DHL} Data-to-Pad HIGH to LOW	2.5		2.8		3.2		3.8		5.3		ns
t _{DHLS} Data-to-Pad HIGH to LOW—low slew	9.0		10.4		11.8		13.8		19.4		ns
t _{ENZL} Enable-to-Pad, Z to L	2.2		2.6		2.9		3.4		4.8		ns
t _{ENZLS} Enable-to-Pad, Z to L—low slew	15.8		18.9		21.3		25.4		34.9		ns
t _{ENZH} Enable-to-Pad, Z to H	2.9		3.3		3.7		4.4		6.2		ns
t _{ENLZ} Enable-to-Pad, L to Z	2.9		3.3		3.7		4.4		6.2		ns
t _{ENHZ} Enable-to-Pad, H to Z	2.5		2.8		3.2		3.8		5.3		ns
d _{TLH} Delta LOW to HIGH	0.025		0.03		0.03		0.04		0.045		ns/pF
d _{THL} Delta HIGH to LOW	0.015		0.015		0.015		0.015		0.025		ns/pF
d _{THLS} Delta HIGH to LOW—low slew	0.053		0.053		0.067		0.073		0.107		ns/pF

Notes:

1. Delays based on 10 pF loading and 25Ω resistance.
2. Delays based on 35 pF loading.

A54SX72A Timing Characteristics (Continued)

 (Worst-Case Commercial Conditions $V_{CCA} = 2.3V$, $V_{CCI} = 4.75V$, $T_J = 70^\circ C$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		'-F' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5.0V PCI Output Module Timing¹												
t _{DLH}	Data-to-Pad LOW to HIGH	2.1	2.5	2.8	3.3	4.6	ns					
t _{DHL}	Data-to-Pad HIGH to LOW	2.7	3.1	3.5	4.2	5.8	ns					
t _{DHLS}	Data-to-Pad HIGH to LOW—low slew	7.4	8.5	9.6	11.3	15.9	ns					
t _{ENZL}	Enable-to-Pad, Z to L	1.3	1.5	1.7	2.0	2.8	ns					
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	3.5	5.1	5.9	6.9	9.7	ns					
t _{ENZH}	Enable-to-Pad, Z to H	1.3	1.5	1.7	2.0	2.8	ns					
t _{ENLZ}	Enable-to-Pad, L to Z	3.0	3.5	3.9	4.6	6.4	ns					
t _{ENHZ}	Enable-to-Pad, H to Z	3.0	3.5	3.9	4.6	6.4	ns					
d _{TLH}	Delta LOW to HIGH	0.016	0.016	0.02	0.022	0.032	ns/pF					
d _{THL}	Delta HIGH to LOW	0.026	0.03	0.032	0.04	0.052	ns/pF					
d _{THLS}	Delta HIGH to LOW—low slew	0.04	0.052	0.06	0.07	0.096	ns/pF					
5.0V TTL Output Module Timing²												
t _{DLH}	Data-to-Pad LOW to HIGH	1.9	2.2	2.5	3.0	4.2	ns					
t _{DHL}	Data-to-Pad HIGH to LOW	2.5	2.9	3.3	3.9	5.4	ns					
t _{DHLS}	Data-to-Pad HIGH to LOW—low slew	6.6	7.6	8.6	10.2	14.2	ns					
t _{ENZL}	Enable-to-Pad, Z to L	2.1	2.4	2.7	3.2	4.5	ns					
t _{ENZLS}	Enable-to-Pad, Z to L—low slew	7.4	8.4	9.5	11.0	15.4	ns					
t _{ENZH}	Enable-to-Pad, Z to H	2.3	2.7	3.1	3.6	5.0	ns					
t _{ENLZ}	Enable-to-Pad, L to Z	3.6	4.2	4.7	5.6	7.8	ns					
t _{ENHZ}	Enable-to-Pad, H to Z	3.0	3.5	3.9	4.6	6.4	ns					
d _{TLH}	Delta LOW to HIGH	0.014	0.017	0.017	0.023	0.031	ns/pF					
d _{THL}	Delta HIGH to LOW	0.023	0.029	0.031	0.037	0.051	ns/pF					
d _{THLS}	Delta HIGH to LOW—low slew	0.043	0.046	0.057	0.066	0.089	ns/pF					

Notes:

1. Delays based on 50 pF loading.
2. Delays based on 35 pF loading.

Pin Description

CLKA/B Clock A and B

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, 3.3V PCI or 5V PCI specifications. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board except A54SX72A. In A54SX72A these clocks can be configured as user I/O.

QCLKA/B/C/D, Quadrant Clock A, B, C, and D I/O

These four pins are the quadrant clock inputs and are only for A54SX72A with A, B, C, and D corresponding to bottom-left, bottom-right, top-left, and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTTL, 3.3V PCI or 5V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. If not used as a clock it will behave as a regular I/O.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hardwired) Array Clock

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTTL, 3.3V PCI or 5V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTTL, 3.3V PCI or 5V PCI specifications. Unused I/O pins are automatically tristated by the Designer Series software.

NC No Connection

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device. The only exception is for the A54SX32A FG-484, where the NC pins must be left floating.

PRA, I/O Probe A/B

PRB, I/O

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe

capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O Test Clock

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to [Table 5 on page 11](#)). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O Test Data Input

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to [Table 5 on page 11](#)). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to [Table 5 on page 11](#)). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the "checksum" command is run. It will return to user IO when "checksum" is complete.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to [Table 5 on page 11](#)). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O Boundary Scan Reset Pin

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active-low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the "Reserve JTAG Reset Pin" is not selected in Designer.

V_{CCI} Supply Voltage

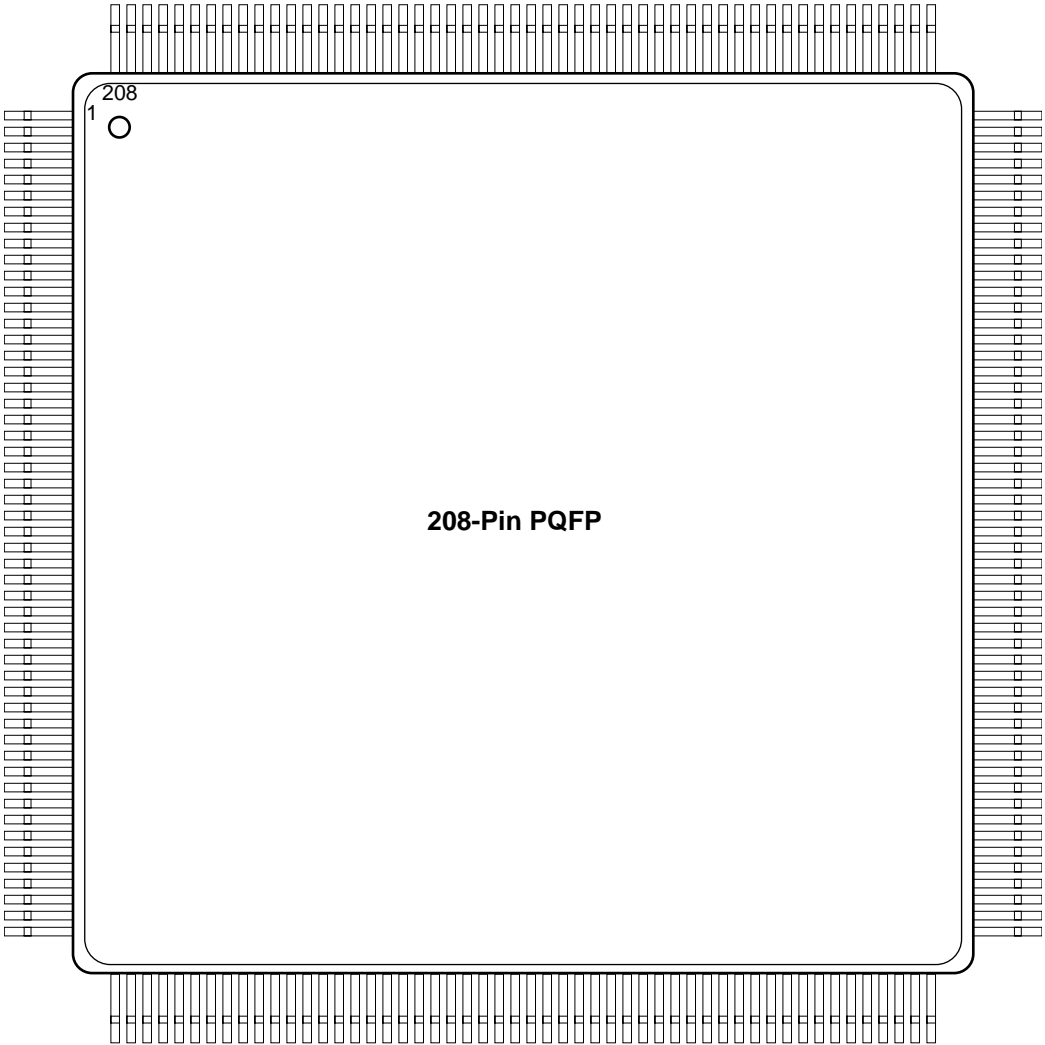
Supply voltage for I/Os. See "Recommended Operating Conditions" table on page 14. All V_{CCI} power pins in the device should be connected.

V_{CCA} Supply Voltage

Supply voltage for Array. See "Recommended Operating Conditions" table on page 14. All V_{CCA} power pins in the device should be connected.

Package Pin Assignments

208-Pin PQFP (Top View)



208-Pin PQFP

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
1	GND	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O	I/O
4	NC	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O
6	NC	I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O
11	TMS	TMS	TMS	TMS
12	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
13	I/O	I/O	I/O	I/O
14	NC	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O
17	NC	I/O	I/O	I/O
18	I/O	I/O	I/O	GND
19	I/O	I/O	I/O	V _{CCA}
20	NC	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	I/O	I/O	I/O
23	NC	I/O	I/O	I/O
24	I/O	I/O	I/O	I/O
25	NC	NC	NC	I/O
26	GND	GND	GND	GND
27	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
28	GND	GND	GND	GND
29	I/O	I/O	I/O	I/O
30	TRST, I/O	TRST, I/O	TRST, I/O	TRST, I/O
31	NC	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	I/O	I/O	I/O	I/O
34	I/O	I/O	I/O	I/O
35	NC	I/O	I/O	I/O
36	I/O	I/O	I/O	I/O
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	I/O
39	NC	I/O	I/O	I/O
40	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
41	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
42	I/O	I/O	I/O	I/O
43	I/O	I/O	I/O	I/O
44	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O
46	I/O	I/O	I/O	I/O

208-Pin PQFP (Continued)

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
47	I/O	I/O	I/O	I/O
48	NC	I/O	I/O	I/O
49	I/O	I/O	I/O	I/O
50	NC	I/O	I/O	I/O
51	I/O	I/O	I/O	I/O
52	GND	GND	GND	GND
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
61	NC	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O
63	I/O	I/O	I/O	I/O
64	NC	I/O	I/O	I/O
65	I/O	I/O	NC	I/O
66	I/O	I/O	I/O	I/O
67	NC	I/O	I/O	I/O
68	I/O	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	NC	I/O	I/O	I/O
71	I/O	I/O	I/O	I/O
72	I/O	I/O	I/O	I/O
73	NC	I/O	I/O	I/O
74	I/O	I/O	I/O	QCLKA
75	NC	I/O	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O	PRB, I/O
77	GND	GND	GND	GND
78	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
79	GND	GND	GND	GND
80	NC	NC	NC	NC
81	I/O	I/O	I/O	I/O
82	HCLK	HCLK	HCLK	HCLK
83	I/O	I/O	I/O	V _{CCI}
84	I/O	I/O	I/O	QCLKB
85	NC	I/O	I/O	I/O
86	I/O	I/O	I/O	I/O
87	I/O	I/O	I/O	I/O
88	NC	I/O	I/O	I/O
89	I/O	I/O	I/O	I/O
90	I/O	I/O	I/O	I/O
91	NC	I/O	I/O	I/O
92	I/O	I/O	I/O	I/O

208-Pin PQFP (Continued)

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
93	I/O	I/O	I/O	I/O
94	NC	I/O	I/O	I/O
95	I/O	I/O	I/O	I/O
96	I/O	I/O	I/O	I/O
97	NC	I/O	I/O	I/O
98	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
99	I/O	I/O	I/O	I/O
100	I/O	I/O	I/O	I/O
101	I/O	I/O	I/O	I/O
102	I/O	I/O	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O	TDO, I/O
104	I/O	I/O	I/O	I/O
105	GND	GND	GND	GND
106	NC	I/O	I/O	I/O
107	I/O	I/O	I/O	I/O
108	NC	I/O	I/O	I/O
109	I/O	I/O	I/O	I/O
110	I/O	I/O	I/O	I/O
111	I/O	I/O	I/O	I/O
112	I/O	I/O	I/O	I/O
113	I/O	I/O	I/O	I/O
114	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
115	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
116	NC	I/O	I/O	GND
117	I/O	I/O	I/O	V _{CCA}
118	I/O	I/O	I/O	I/O
119	NC	I/O	I/O	I/O
120	I/O	I/O	I/O	I/O
121	I/O	I/O	I/O	I/O
122	NC	I/O	I/O	I/O
123	I/O	I/O	I/O	I/O
124	I/O	I/O	I/O	I/O
125	NC	I/O	I/O	I/O
126	I/O	I/O	I/O	I/O
127	I/O	I/O	I/O	I/O
128	I/O	I/O	I/O	I/O
129	GND	GND	GND	GND
130	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
131	GND	GND	GND	GND
132	NC	NC	NC	I/O
133	I/O	I/O	I/O	I/O
134	I/O	I/O	I/O	I/O
135	NC	I/O	I/O	I/O
136	I/O	I/O	I/O	I/O
137	I/O	I/O	I/O	I/O
138	NC	I/O	I/O	I/O

208-Pin PQFP (Continued)

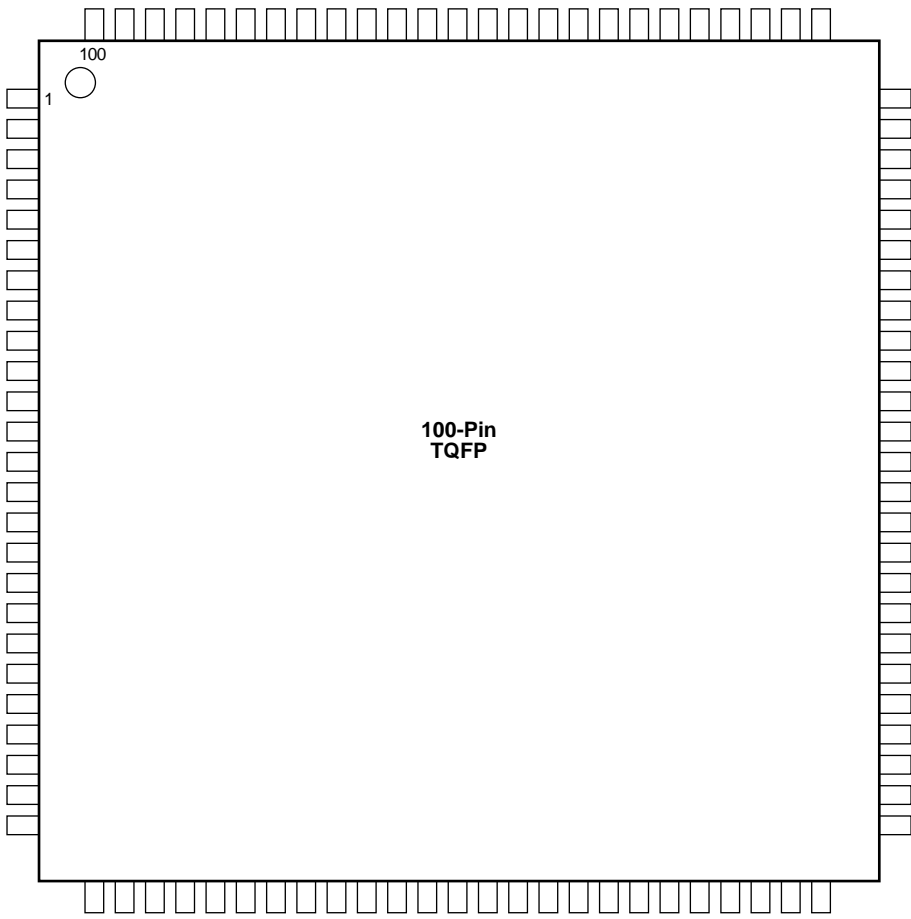
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
139	I/O	I/O	I/O	I/O
140	I/O	I/O	I/O	I/O
141	NC	I/O	I/O	I/O
142	I/O	I/O	I/O	I/O
143	NC	I/O	I/O	I/O
144	I/O	I/O	I/O	I/O
145	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}
146	GND	GND	GND	GND
147	I/O	I/O	I/O	I/O
148	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
149	I/O	I/O	I/O	I/O
150	I/O	I/O	I/O	I/O
151	I/O	I/O	I/O	I/O
152	I/O	I/O	I/O	I/O
153	I/O	I/O	I/O	I/O
154	I/O	I/O	I/O	I/O
155	NC	I/O	I/O	I/O
156	NC	I/O	I/O	I/O
157	GND	GND	GND	GND
158	I/O	I/O	I/O	I/O
159	I/O	I/O	I/O	I/O
160	I/O	I/O	I/O	I/O
161	I/O	I/O	I/O	I/O
162	I/O	I/O	I/O	I/O
163	I/O	I/O	I/O	I/O
164	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
165	I/O	I/O	I/O	I/O
166	I/O	I/O	I/O	I/O
167	NC	I/O	I/O	I/O
168	I/O	I/O	I/O	I/O
169	I/O	I/O	I/O	I/O
170	NC	I/O	I/O	I/O
171	I/O	I/O	I/O	I/O
172	I/O	I/O	I/O	I/O
173	NC	I/O	I/O	I/O
174	I/O	I/O	I/O	I/O
175	I/O	I/O	I/O	I/O
176	NC	I/O	I/O	I/O
177	I/O	I/O	I/O	I/O
178	I/O	I/O	I/O	QCLKD
179	I/O	I/O	I/O	I/O
180	CLKA	CLKA	CLKA	CLKA
181	CLKB	CLKB	CLKB	CLKB
182	NC	NC	NC	NC
183	GND	GND	GND	GND
184	V _{CCA}	V _{CCA}	V _{CCA}	V _{CCA}

208-Pin PQFP (Continued)

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
185	GND	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O	V _{CCI}
188	I/O	I/O	I/O	I/O
189	NC	I/O	I/O	I/O
190	I/O	I/O	I/O	QCLKC
191	I/O	I/O	I/O	I/O
192	NC	I/O	I/O	I/O
193	I/O	I/O	I/O	I/O
194	I/O	I/O	I/O	I/O
195	NC	I/O	I/O	I/O
196	I/O	I/O	I/O	I/O
197	I/O	I/O	I/O	I/O
198	NC	I/O	I/O	I/O
199	I/O	I/O	I/O	I/O
200	I/O	I/O	I/O	I/O
201	V _{CCI}	V _{CCI}	V _{CCI}	V _{CCI}
202	NC	I/O	I/O	I/O
203	NC	I/O	I/O	I/O
204	I/O	I/O	I/O	I/O
205	NC	I/O	I/O	I/O
206	I/O	I/O	I/O	I/O
207	I/O	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O	TCK, I/O

Package Pin Assignments (Continued)

100-Pin TQFP (Top View)



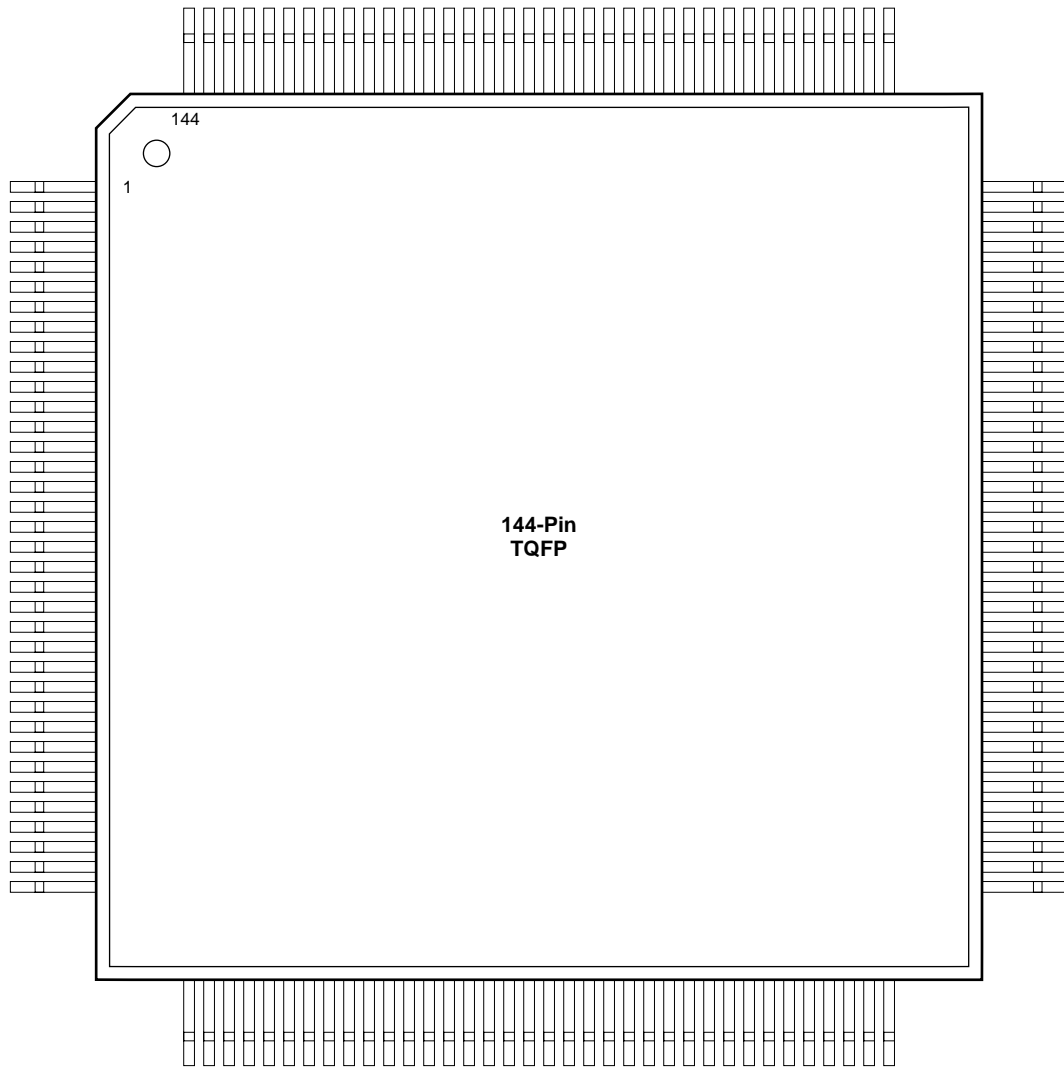
100-TQFP

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	TMS	TMS	TMS
8	V _{CCI}	V _{CCI}	V _{CCI}
9	GND	GND	GND
10	I/O	I/O	I/O
11	I/O	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	TRST, I/O	TRST, I/O	TRST, I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	V _{CCI}	V _{CCI}	V _{CCI}
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	V _{CCA}	V _{CCA}	V _{CCA}
36	GND	GND	GND
37	NC	NC	NC
38	I/O	I/O	I/O
39	HCLK	HCLK	HCLK
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V _{CCI}	V _{CCI}	V _{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	TDO, I/O	TDO, I/O	TDO, I/O
50	I/O	I/O	I/O

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
51	GND	GND	GND
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	V _{CCA}	V _{CCA}	V _{CCA}
58	V _{CCI}	V _{CCI}	V _{CCI}
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	V _{CCA}	V _{CCA}	V _{CCA}
68	GND	GND	GND
69	GND	GND	GND
70	I/O	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	V _{CCI}	V _{CCI}	V _{CCI}
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	V _{CCA}	V _{CCA}	V _{CCA}
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

Package Pin Assignments (continued)

144-Pin TQFP (Top View)



144-Pin TQFP

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	TMS	TMS	TMS
10	V _{CCI}	V _{CCI}	V _{CCI}
11	GND	GND	GND
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	NC	NC	NC
20	V _{CCA}	V _{CCA}	V _{CCA}
21	I/O	I/O	I/O
22	TRST, I/O	TRST, I/O	TRST, I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	GND	GND	GND
29	V _{CCI}	V _{CCI}	V _{CCI}
30	V _{CCA}	V _{CCA}	V _{CCA}
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	GND	GND	GND
37	I/O	I/O	I/O
38	I/O	I/O	I/O

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V _{CCI}	V _{CCI}	V _{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	PRB, I/O	PRB, I/O	PRB, I/O
55	I/O	I/O	I/O
56	V _{CCA}	V _{CCA}	V _{CCA}
57	GND	GND	GND
58	NC	NC	NC
59	I/O	I/O	I/O
60	HCLK	HCLK	HCLK
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	V _{CCI}	V _{CCI}	V _{CCI}
69	I/O	I/O	I/O
70	I/O	I/O	I/O
71	TDO, I/O	TDO, I/O	TDO, I/O
72	I/O	I/O	I/O
73	GND	GND	GND
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O

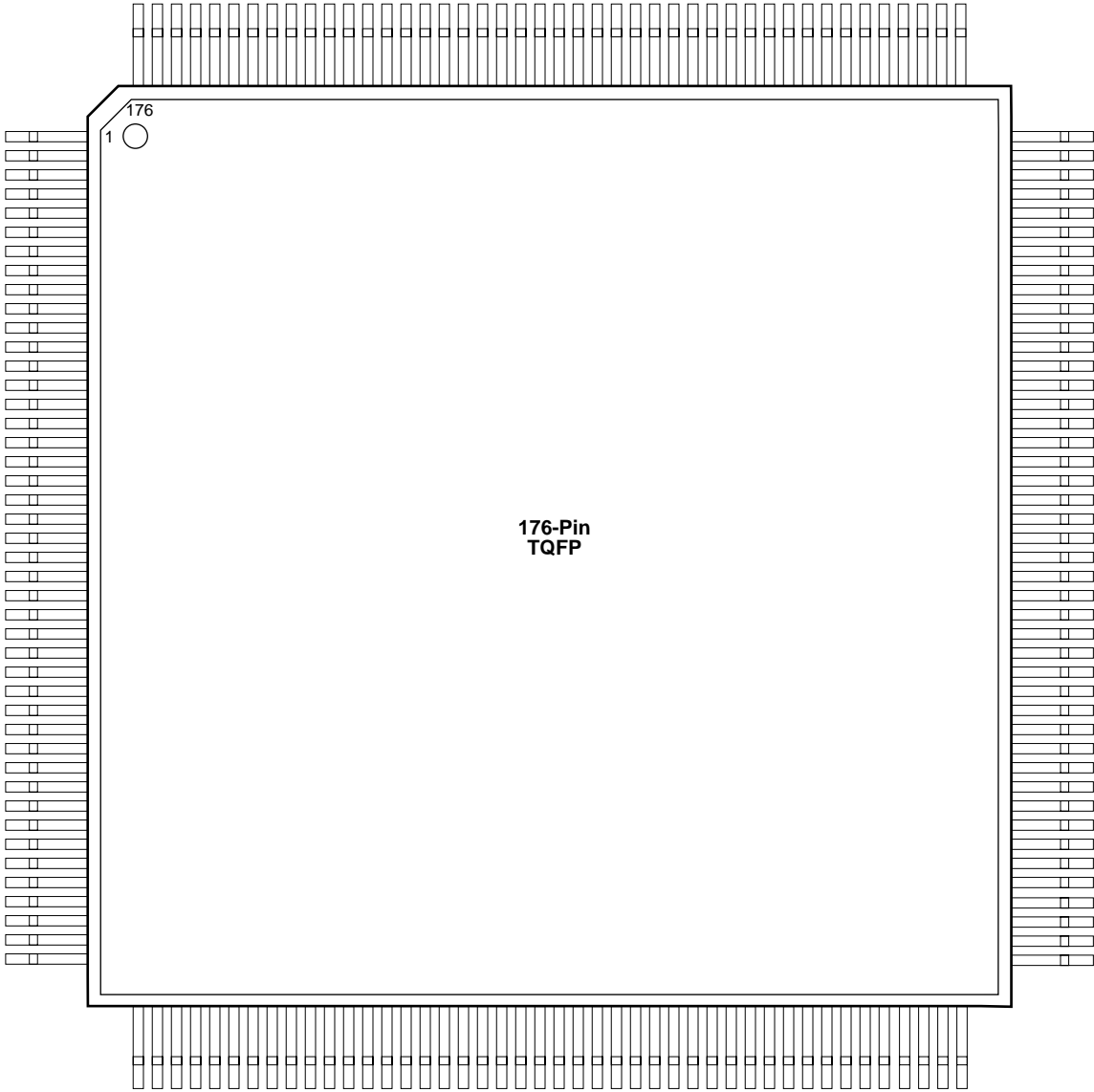
144-Pin TQFP (Continued)

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	V _{CCA}	V _{CCA}	V _{CCA}
80	V _{CCI}	V _{CCI}	V _{CCI}
81	GND	GND	GND
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	V _{CCA}	V _{CCA}	V _{CCA}
90	NC	NC	NC
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V _{CCA}	V _{CCA}	V _{CCA}
99	GND	GND	GND
100	I/O	I/O	I/O
101	GND	GND	GND
102	V _{CCI}	V _{CCI}	V _{CCI}
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	I/O	I/O	I/O
109	GND	GND	GND
110	I/O	I/O	I/O

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	V _{CCI}	V _{CCI}	V _{CCI}
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	CLKA	CLKA	CLKA
126	CLKB	CLKB	CLKB
127	NC	NC	NC
128	GND	GND	GND
129	V _{CCA}	V _{CCA}	V _{CCA}
130	I/O	I/O	I/O
131	PRA, I/O	PRA, I/O	PRA, I/O
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V _{CCI}	V _{CCI}	V _{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	TCK, I/O	TCK, I/O	TCK, I/O

Package Pin Assignments (Continued)

176-Pin TQFP (Top View)

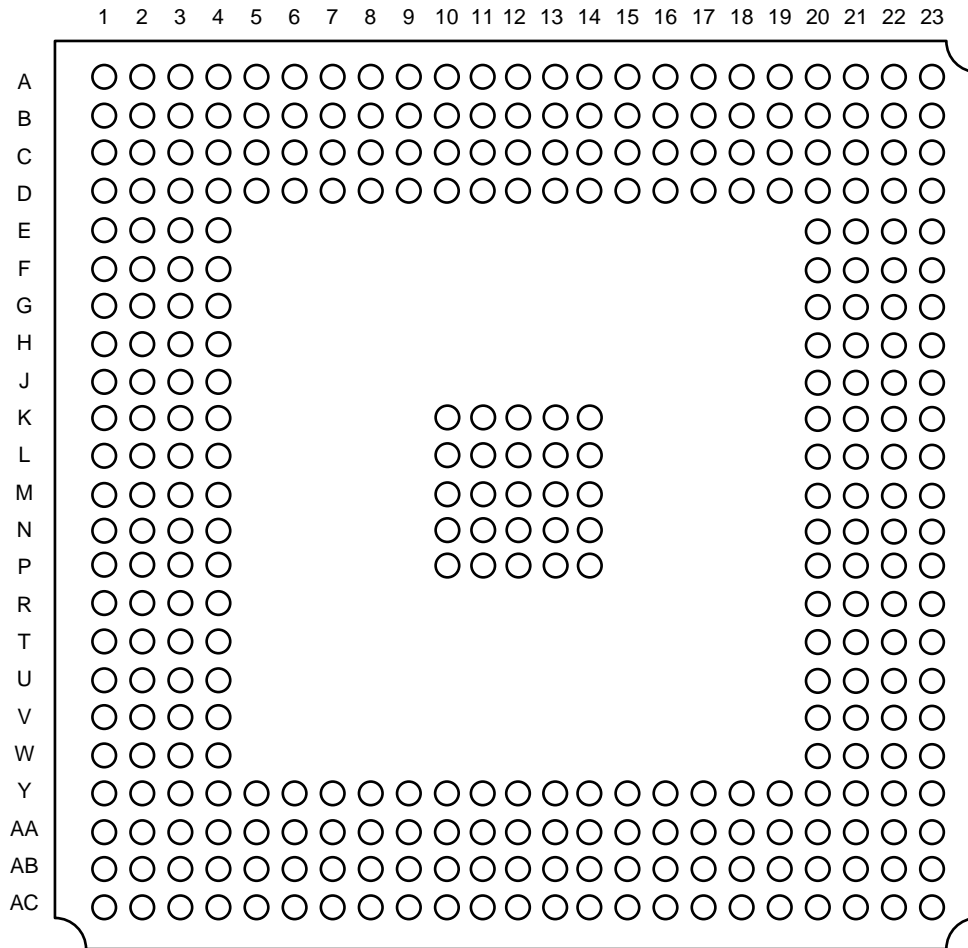


176-Pin TQFP

Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function
1	GND	46	I/O	91	I/O	136	I/O
2	TDI, I/O	47	I/O	92	I/O	137	I/O
3	I/O	48	I/O	93	I/O	138	I/O
4	I/O	49	I/O	94	I/O	139	I/O
5	I/O	50	I/O	95	I/O	140	V _{CCI}
6	I/O	51	I/O	96	I/O	141	I/O
7	I/O	52	V _{CCI}	97	I/O	142	I/O
8	I/O	53	I/O	98	V _{CCA}	143	I/O
9	I/O	54	I/O	99	V _{CCI}	144	I/O
10	TMS	55	I/O	100	I/O	145	I/O
11	V _{CCI}	56	I/O	101	I/O	146	I/O
12	I/O	57	I/O	102	I/O	147	I/O
13	I/O	58	I/O	103	I/O	148	I/O
14	I/O	59	I/O	104	I/O	149	I/O
15	I/O	60	I/O	105	I/O	150	I/O
16	I/O	61	I/O	106	I/O	151	I/O
17	I/O	62	I/O	107	I/O	152	CLKA
18	I/O	63	I/O	108	GND	153	CLKB
19	I/O	64	PRB, I/O	109	V _{CCA}	154	NC
20	I/O	65	GND	110	GND	155	GND
21	GND	66	V _{CCA}	111	I/O	156	V _{CCA}
22	V _{CCA}	67	NC	112	I/O	157	PRA, I/O
23	GND	68	I/O	113	I/O	158	I/O
24	I/O	69	HCLK	114	I/O	159	I/O
25	TRST, I/O	70	I/O	115	I/O	160	I/O
26	I/O	71	I/O	116	I/O	161	I/O
27	I/O	72	I/O	117	I/O	162	I/O
28	I/O	73	I/O	118	I/O	163	I/O
29	I/O	74	I/O	119	I/O	164	I/O
30	I/O	75	I/O	120	I/O	165	I/O
31	I/O	76	I/O	121	I/O	166	I/O
32	V _{CCI}	77	I/O	122	V _{CCA}	167	I/O
33	V _{CCA}	78	I/O	123	GND	168	I/O
34	I/O	79	I/O	124	V _{CCI}	169	V _{CCI}
35	I/O	80	I/O	125	I/O	170	I/O
36	I/O	81	I/O	126	I/O	171	I/O
37	I/O	82	V _{CCI}	127	I/O	172	I/O
38	I/O	83	I/O	128	I/O	173	I/O
39	I/O	84	I/O	129	I/O	174	I/O
40	I/O	85	I/O	130	I/O	175	I/O
41	I/O	86	I/O	131	I/O	176	TCK, I/O
42	I/O	87	TDO, I/O	132	I/O		
43	I/O	88	I/O	133	GND		
44	GND	89	GND	134	I/O		
45	I/O	90	I/O	135	I/O		

Package Pin Assignments (Continued)

329-Pin PBGA (Top View)



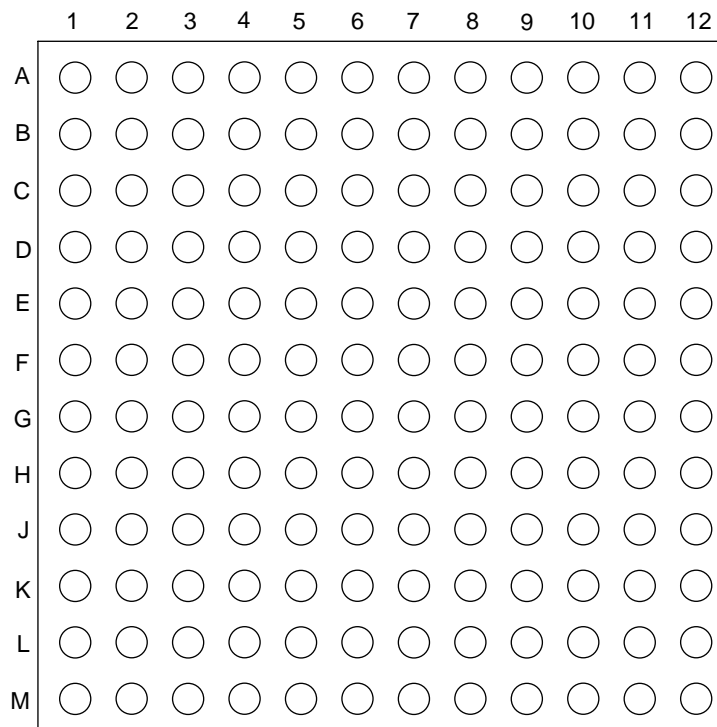
329-Pin PBGA

Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function
A1	GND	AA23	V _{CCI}	AC22	V _{CCI}	C21	V _{CCI}
A2	GND	AB1	I/O	AC23	GND	C22	GND
A3	V _{CCI}	AB2	GND	B1	V _{CCI}	C23	NC
A4	NC	AB3	I/O	B2	GND	D1	I/O
A5	I/O	AB4	I/O	B3	I/O	D2	I/O
A6	I/O	AB5	I/O	B4	I/O	D3	I/O
A7	V _{CCI}	AB6	I/O	B5	I/O	D4	TCK, I/O
A8	NC	AB7	I/O	B6	I/O	D5	I/O
A9	I/O	AB8	I/O	B7	I/O	D6	I/O
A10	I/O	AB9	I/O	B8	I/O	D7	I/O
A11	I/O	AB10	I/O	B9	I/O	D8	I/O
A12	I/O	AB11	PRB, I/O	B10	I/O	D9	I/O
A13	CLKB	AB12	I/O	B11	I/O	D10	I/O
A14	I/O	AB13	HCLK	B12	PRA, I/O	D11	V _{CCA}
A15	I/O	AB14	I/O	B13	CLKA	D12	NC
A16	I/O	AB15	I/O	B14	I/O	D13	I/O
A17	I/O	AB16	I/O	B15	I/O	D14	I/O
A18	I/O	AB17	I/O	B16	I/O	D15	I/O
A19	I/O	AB18	I/O	B17	I/O	D16	I/O
A20	I/O	AB19	I/O	B18	I/O	D17	I/O
A21	NC	AB20	I/O	B19	I/O	D18	I/O
A22	V _{CCI}	AB21	I/O	B20	I/O	D19	I/O
A23	GND	AB22	GND	B21	I/O	D20	I/O
AA1	V _{CCI}	AB23	I/O	B22	GND	D21	I/O
AA2	I/O	AC1	GND	B23	V _{CCI}	D22	I/O
AA3	GND	AC2	V _{CCI}	C1	NC	D23	I/O
AA4	I/O	AC3	NC	C2	TDI, I/O	E1	V _{CCI}
AA5	I/O	AC4	I/O	C3	GND	E2	I/O
AA6	I/O	AC5	I/O	C4	I/O	E3	I/O
AA7	I/O	AC6	I/O	C5	I/O	E4	I/O
AA8	I/O	AC7	I/O	C6	I/O	E20	I/O
AA9	I/O	AC8	I/O	C7	I/O	E21	I/O
AA10	I/O	AC9	V _{CCI}	C8	I/O	E22	I/O
AA11	I/O	AC10	I/O	C9	I/O	E23	I/O
AA12	I/O	AC11	I/O	C10	I/O	F1	I/O
AA13	I/O	AC12	I/O	C11	I/O	F2	TMS
AA14	I/O	AC13	I/O	C12	I/O	F3	I/O
AA15	I/O	AC14	I/O	C13	I/O	F4	I/O
AA16	I/O	AC15	NC	C14	I/O	F20	I/O
AA17	I/O	AC16	I/O	C15	I/O	F21	I/O
AA18	I/O	AC17	I/O	C16	I/O	F22	I/O
AA19	I/O	AC18	I/O	C17	I/O	F23	I/O
AA20	TDO, I/O	AC19	I/O	C18	I/O	G1	I/O
AA21	V _{CCI}	AC20	I/O	C19	I/O	G2	I/O
AA22	I/O	AC21	NC	C20	I/O	G3	I/O

329-Pin PBGA (Continued)

Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function	Pin Number	A54SX32A Function
G4	I/O	L20	NC	R1	I/O	Y4	GND
G20	I/O	L21	I/O	R2	I/O	Y5	I/O
G21	I/O	L22	I/O	R3	I/O	Y6	I/O
G22	I/O	L23	NC	R4	I/O	Y7	I/O
G23	GND	M1	I/O	R20	I/O	Y8	I/O
H1	I/O	M2	I/O	R21	I/O	Y9	I/O
H2	I/O	M3	I/O	R22	I/O	Y10	I/O
H3	I/O	M4	V _{CCA}	R23	I/O	Y11	I/O
H4	I/O	M10	GND	T1	I/O	Y12	V _{CCA}
H20	V _{CCA}	M11	GND	T2	I/O	Y13	NC
H21	I/O	M12	GND	T3	I/O	Y14	I/O
H22	I/O	M13	GND	T4	I/O	Y15	I/O
H23	I/O	M14	GND	T20	I/O	Y16	I/O
J1	NC	M20	V _{CCA}	T21	I/O	Y17	I/O
J2	I/O	M21	I/O	T22	I/O	Y18	I/O
J3	I/O	M22	I/O	T23	I/O	Y19	I/O
J4	I/O	M23	V _{CCI}	U1	I/O	Y20	GND
J20	I/O	N1	I/O	U2	I/O	Y21	I/O
J21	I/O	N2	TRST, I/O	U3	V _{CCA}	Y22	I/O
J22	I/O	N3	I/O	U4	I/O	Y23	I/O
J23	I/O	N4	I/O	U20	I/O		
K1	I/O	N10	GND	U21	V _{CCA}		
K2	I/O	N11	GND	U22	I/O		
K3	I/O	N12	GND	U23	I/O		
K4	I/O	N13	GND	V1	V _{CCI}		
K10	GND	N14	GND	V2	I/O		
K11	GND	N20	NC	V3	I/O		
K12	GND	N21	I/O	V4	I/O		
K13	GND	N22	I/O	V20	I/O		
K14	GND	N23	I/O	V21	I/O		
K20	I/O	P1	I/O	V22	I/O		
K21	I/O	P2	I/O	V23	I/O		
K22	I/O	P3	I/O	W1	I/O		
K23	I/O	P4	I/O	W2	I/O		
L1	I/O	P10	GND	W3	I/O		
L2	I/O	P11	GND	W4	I/O		
L3	I/O	P12	GND	W20	I/O		
L4	NC	P13	GND	W21	I/O		
L10	GND	P14	GND	W22	I/O		
L11	GND	P20	I/O	W23	NC		
L12	GND	P21	I/O	Y1	NC		
L13	GND	P22	I/O	Y2	I/O		
L14	GND	P23	I/O	Y3	I/O		

Package Pin Assignments (Continued)
144-Pin FBGA (Top View)



144-Pin FBGA

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
A1	I/O	I/O	I/O
A2	I/O	I/O	I/O
A3	I/O	I/O	I/O
A4	I/O	I/O	I/O
A5	V _{CCA}	V _{CCA}	V _{CCA}
A6	GND	GND	GND
A7	CLKA	CLKA	CLKA
A8	I/O	I/O	I/O
A9	I/O	I/O	I/O
A10	I/O	I/O	I/O
A11	I/O	I/O	I/O
A12	I/O	I/O	I/O
B1	I/O	I/O	I/O
B2	GND	GND	GND
B3	I/O	I/O	I/O
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	I/O	I/O	I/O
B7	CLKB	CLKB	CLKB
B8	I/O	I/O	I/O
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	GND	GND	GND
B12	I/O	I/O	I/O
C1	I/O	I/O	I/O
C2	I/O	I/O	I/O
C3	TCK, I/O	TCK, I/O	TCK, I/O
C4	I/O	I/O	I/O
C5	I/O	I/O	I/O
C6	PRA, I/O	PRA, I/O	PRA, I/O
C7	I/O	I/O	I/O
C8	I/O	I/O	I/O
C9	I/O	I/O	I/O
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O
D1	I/O	I/O	I/O
D2	V _{CCI}	V _{CCI}	V _{CCI}

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
D3	TDI, I/O	TDI, I/O	TDI, I/O
D4	I/O	I/O	I/O
D5	I/O	I/O	I/O
D6	I/O	I/O	I/O
D7	I/O	I/O	I/O
D8	I/O	I/O	I/O
D9	I/O	I/O	I/O
D10	I/O	I/O	I/O
D11	I/O	I/O	I/O
D12	I/O	I/O	I/O
E1	I/O	I/O	I/O
E2	I/O	I/O	I/O
E3	I/O	I/O	I/O
E4	I/O	I/O	I/O
E5	TMS	TMS	TMS
E6	V _{CCI}	V _{CCI}	V _{CCI}
E7	V _{CCI}	V _{CCI}	V _{CCI}
E8	V _{CCI}	V _{CCI}	V _{CCI}
E9	V _{CCA}	V _{CCA}	V _{CCA}
E10	I/O	I/O	I/O
E11	GND	GND	GND
E12	I/O	I/O	I/O
F1	I/O	I/O	I/O
F2	I/O	I/O	I/O
F3	NC	NC	NC
F4	I/O	I/O	I/O
F5	GND	GND	GND
F6	GND	GND	GND
F7	GND	GND	GND
F8	V _{CCI}	V _{CCI}	V _{CCI}
F9	I/O	I/O	I/O
F10	GND	GND	GND
F11	I/O	I/O	I/O
F12	I/O	I/O	I/O
G1	I/O	I/O	I/O
G2	GND	GND	GND
G3	I/O	I/O	I/O
G4	I/O	I/O	I/O

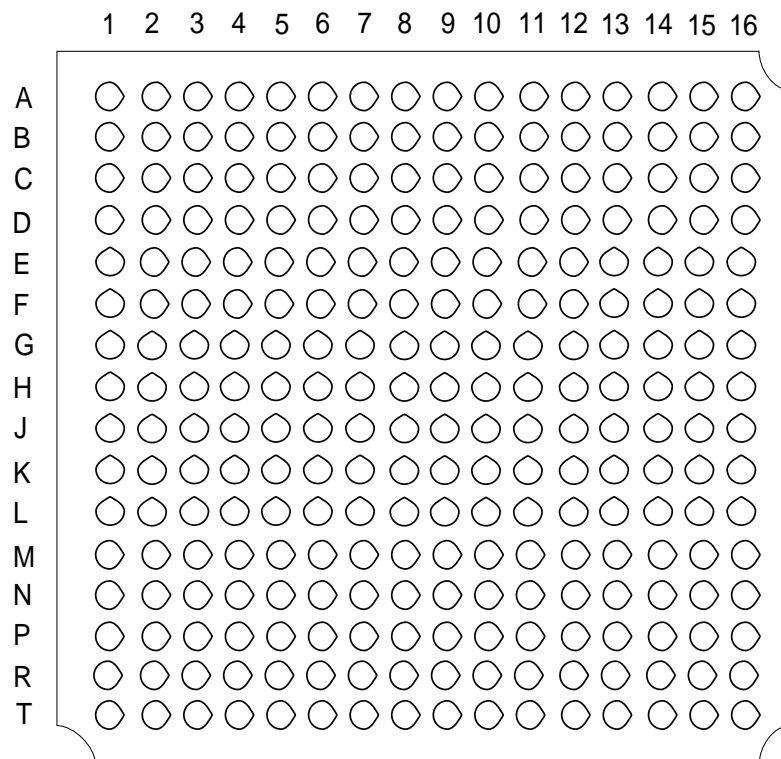
144-Pin FBGA (Continued)

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
G5	GND	GND	GND
G6	GND	GND	GND
G7	GND	GND	GND
G8	V _{CCI}	V _{CCI}	V _{CCI}
G9	I/O	I/O	I/O
G10	I/O	I/O	I/O
G11	I/O	I/O	I/O
G12	I/O	I/O	I/O
H1	TRST, I/O	TRST, I/O	TRST, I/O
H2	I/O	I/O	I/O
H3	I/O	I/O	I/O
H4	I/O	I/O	I/O
H5	V _{CCA}	V _{CCA}	V _{CCA}
H6	V _{CCA}	V _{CCA}	V _{CCA}
H7	V _{CCI}	V _{CCI}	V _{CCI}
H8	V _{CCI}	V _{CCI}	V _{CCI}
H9	V _{CCA}	V _{CCA}	V _{CCA}
H10	I/O	I/O	I/O
H11	I/O	I/O	I/O
H12	NC	NC	NC
J1	I/O	I/O	I/O
J2	I/O	I/O	I/O
J3	I/O	I/O	I/O
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J6	PRB, I/O	PRB, I/O	PRB, I/O
J7	I/O	I/O	I/O
J8	I/O	I/O	I/O
J9	I/O	I/O	I/O
J10	I/O	I/O	I/O
J11	I/O	I/O	I/O
J12	V _{CCA}	V _{CCA}	V _{CCA}
K1	I/O	I/O	I/O
K2	I/O	I/O	I/O

Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
K3	I/O	I/O	I/O
K4	I/O	I/O	I/O
K5	I/O	I/O	I/O
K6	I/O	I/O	I/O
K7	GND	GND	GND
K8	I/O	I/O	I/O
K9	I/O	I/O	I/O
K10	GND	GND	GND
K11	I/O	I/O	I/O
K12	I/O	I/O	I/O
L1	GND	GND	GND
L2	I/O	I/O	I/O
L3	I/O	I/O	I/O
L4	I/O	I/O	I/O
L5	I/O	I/O	I/O
L6	I/O	I/O	I/O
L7	HCLK	HCLK	HCLK
L8	I/O	I/O	I/O
L9	I/O	I/O	I/O
L10	I/O	I/O	I/O
L11	I/O	I/O	I/O
L12	I/O	I/O	I/O
M1	I/O	I/O	I/O
M2	I/O	I/O	I/O
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O
M5	I/O	I/O	I/O
M6	I/O	I/O	I/O
M7	V _{CCA}	V _{CCA}	V _{CCA}
M8	I/O	I/O	I/O
M9	I/O	I/O	I/O
M10	I/O	I/O	I/O
M11	TDO, I/O	TDO, I/O	TDO, I/O
M12	I/O	I/O	I/O

Package Pin Assignments (Continued)

256-Pin FBGA (Top View)



256-Pin FBGA

Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
A1	GND	GND	GND
A2	TCK, I/O	TCK, I/O	TCK, I/O
A3	I/O	I/O	I/O
A4	I/O	I/O	I/O
A5	I/O	I/O	I/O
A6	I/O	I/O	I/O
A7	I/O	I/O	I/O
A8	I/O	I/O	I/O
A9	CLKB	CLKB	CLKB
A10	I/O	I/O	I/O
A11	I/O	I/O	I/O
A12	NC	I/O	I/O
A13	I/O	I/O	I/O
A14	I/O	I/O	I/O
A15	GND	GND	GND
A16	GND	GND	GND
B1	I/O	I/O	I/O
B2	GND	GND	GND
B3	I/O	I/O	I/O
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	NC	I/O	I/O
B7	I/O	I/O	I/O
B8	V _{CCA}	V _{CCA}	V _{CCA}
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	NC	I/O	I/O
B12	I/O	I/O	I/O
B13	I/O	I/O	I/O
B14	I/O	I/O	I/O
B15	GND	GND	GND
B16	I/O	I/O	I/O
C1	I/O	I/O	I/O
C2	TDI, I/O	TDI, I/O	TDI, I/O
C3	GND	GND	GND
C4	I/O	I/O	I/O
C5	NC	I/O	I/O
C6	I/O	I/O	I/O
C7	I/O	I/O	I/O
C8	I/O	I/O	I/O
C9	CLKA	CLKA	CLKA
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O
C13	I/O	I/O	I/O

Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
C14	I/O	I/O	I/O
C15	I/O	I/O	I/O
C16	I/O	I/O	I/O
D1	I/O	I/O	I/O
D2	I/O	I/O	I/O
D3	I/O	I/O	I/O
D4	I/O	I/O	I/O
D5	I/O	I/O	I/O
D6	I/O	I/O	I/O
D7	I/O	I/O	I/O
D8	PRA, I/O	PRA, I/O	PRA, I/O
D9	I/O	I/O	QCLKD
D10	I/O	I/O	I/O
D11	NC	I/O	I/O
D12	I/O	I/O	I/O
D13	I/O	I/O	I/O
D14	I/O	I/O	I/O
D15	I/O	I/O	I/O
D16	I/O	I/O	I/O
E1	I/O	I/O	I/O
E2	I/O	I/O	I/O
E3	I/O	I/O	I/O
E4	I/O	I/O	I/O
E5	I/O	I/O	I/O
E6	I/O	I/O	I/O
E7	I/O	I/O	QCLKC
E8	I/O	I/O	I/O
E9	I/O	I/O	I/O
E10	I/O	I/O	I/O
E11	I/O	I/O	I/O
E12	I/O	I/O	I/O
E13	NC	I/O	I/O
E14	I/O	I/O	I/O
E15	I/O	I/O	I/O
E16	I/O	I/O	I/O
F1	I/O	I/O	I/O
F2	I/O	I/O	I/O
F3	I/O	I/O	I/O
F4	TMS	TMS	TMS
F5	I/O	I/O	I/O
F6	I/O	I/O	I/O
F7	V _{CCI}	V _{CCI}	V _{CCI}
F8	V _{CCI}	V _{CCI}	V _{CCI}
F9	V _{CCI}	V _{CCI}	V _{CCI}
F10	V _{CCI}	V _{CCI}	V _{CCI}

256-Pin FBGA (Continued)

Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
F11	I/O	I/O	I/O
F12	VCCA	VCCA	VCCA
F13	I/O	I/O	I/O
F14	I/O	I/O	I/O
F15	I/O	I/O	I/O
F16	I/O	I/O	I/O
G1	NC	I/O	I/O
G2	I/O	I/O	I/O
G3	NC	I/O	I/O
G4	I/O	I/O	I/O
G5	I/O	I/O	I/O
G6	V _{CCI}	V _{CCI}	V _{CCI}
G7	GND	GND	GND
G8	GND	GND	GND
G9	GND	GND	GND
G10	GND	GND	GND
G11	V _{CCI}	V _{CCI}	V _{CCI}
G12	I/O	I/O	I/O
G13	GND	GND	GND
G14	NC	I/O	I/O
G15	V _{CCA}	V _{CCA}	V _{CCA}
G16	I/O	I/O	I/O
H1	I/O	I/O	I/O
H2	I/O	I/O	I/O
H3	V _{CCA}	V _{CCA}	V _{CCA}
H4	TRST, I/O	TRST, I/O	TRST, I/O
H5	I/O	I/O	I/O
H6	V _{CCI}	V _{CCI}	V _{CCI}
H7	GND	GND	GND
H8	GND	GND	GND
H9	GND	GND	GND
H10	GND	GND	GND
H11	V _{CCI}	V _{CCI}	V _{CCI}
H12	I/O	I/O	I/O
H13	I/O	I/O	I/O
H14	I/O	I/O	I/O
H15	I/O	I/O	I/O
H16	NC	I/O	I/O
J1	NC	I/O	I/O
J2	NC	I/O	I/O
J3	NC	I/O	I/O
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J6	V _{CCI}	V _{CCI}	V _{CCI}
J7	GND	GND	GND

Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
J8	GND	GND	GND
J9	GND	GND	GND
J10	GND	GND	GND
J11	V _{CCI}	V _{CCI}	V _{CCI}
J12	I/O	I/O	I/O
J13	I/O	I/O	I/O
J14	I/O	I/O	I/O
J15	I/O	I/O	I/O
J16	I/O	I/O	I/O
K1	I/O	I/O	I/O
K2	I/O	I/O	I/O
K3	NC	I/O	I/O
K4	V _{CCA}	V _{CCA}	V _{CCA}
K5	I/O	I/O	I/O
K6	V _{CCI}	V _{CCI}	V _{CCI}
K7	GND	GND	GND
K8	GND	GND	GND
K9	GND	GND	GND
K10	GND	GND	GND
K11	V _{CCI}	V _{CCI}	V _{CCI}
K12	I/O	I/O	I/O
K13	I/O	I/O	I/O
K14	I/O	I/O	I/O
K15	NC	I/O	I/O
K16	I/O	I/O	I/O
L1	I/O	I/O	I/O
L2	I/O	I/O	I/O
L3	I/O	I/O	I/O
L4	I/O	I/O	I/O
L5	I/O	I/O	I/O
L6	I/O	I/O	I/O
L7	V _{CCI}	V _{CCI}	V _{CCI}
L8	V _{CCI}	V _{CCI}	V _{CCI}
L9	V _{CCI}	V _{CCI}	V _{CCI}
L10	V _{CCI}	V _{CCI}	V _{CCI}
L11	I/O	I/O	I/O
L12	I/O	I/O	I/O
L13	I/O	I/O	I/O
L14	I/O	I/O	I/O
L15	I/O	I/O	I/O
L16	NC	I/O	I/O
M1	I/O	I/O	I/O
M2	I/O	I/O	I/O
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O

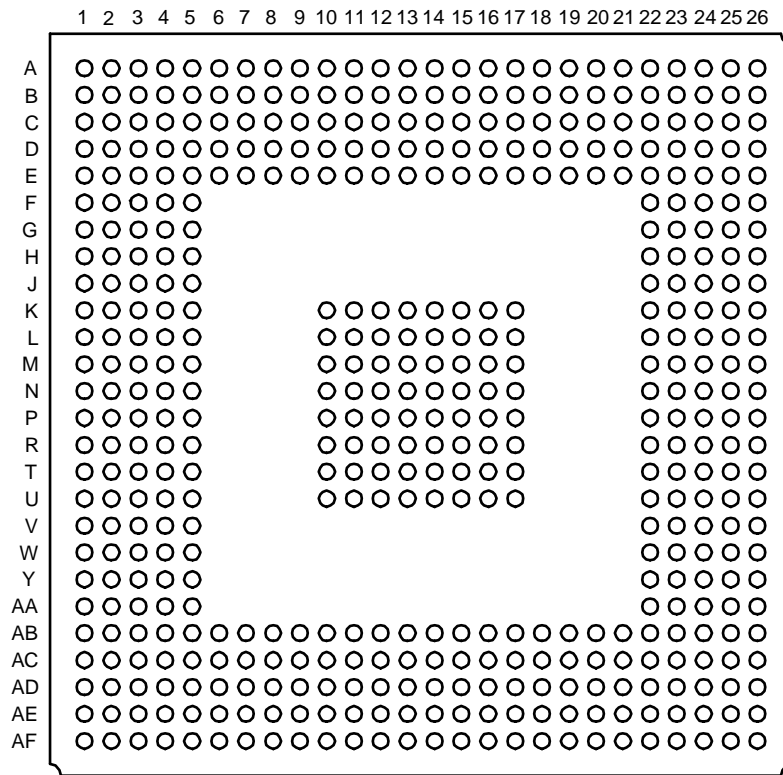
256-Pin FBGA (Continued)

Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
M5	I/O	I/O	I/O
M6	I/O	I/O	I/O
M7	I/O	I/O	QCLKA
M8	PRB, I/O	PRB, I/O	PRB, I/O
M9	I/O	I/O	I/O
M10	I/O	I/O	I/O
M11	I/O	I/O	I/O
M12	NC	I/O	I/O
M13	I/O	I/O	I/O
M14	NC	I/O	I/O
M15	I/O	I/O	I/O
M16	I/O	I/O	I/O
N1	I/O	I/O	I/O
N2	I/O	I/O	I/O
N3	I/O	I/O	I/O
N4	I/O	I/O	I/O
N5	I/O	I/O	I/O
N6	I/O	I/O	I/O
N7	I/O	I/O	I/O
N8	I/O	I/O	I/O
N9	I/O	I/O	I/O
N10	I/O	I/O	I/O
N11	I/O	I/O	I/O
N12	I/O	I/O	I/O
N13	I/O	I/O	I/O
N14	I/O	I/O	I/O
N15	I/O	I/O	I/O
N16	I/O	I/O	I/O
P1	I/O	I/O	I/O
P2	GND	GND	GND
P3	I/O	I/O	I/O
P4	I/O	I/O	I/O
P5	NC	I/O	I/O
P6	I/O	I/O	I/O
P7	I/O	I/O	I/O
P8	I/O	I/O	I/O
P9	I/O	I/O	I/O
P10	NC	I/O	I/O

Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
P11	I/O	I/O	I/O
P12	I/O	I/O	I/O
P13	V _{CCA}	V _{CCA}	V _{CCA}
P14	I/O	I/O	I/O
P15	I/O	I/O	I/O
P16	I/O	I/O	I/O
R1	I/O	I/O	I/O
R2	GND	GND	GND
R3	I/O	I/O	I/O
R4	NC	I/O	I/O
R5	I/O	I/O	I/O
R6	I/O	I/O	I/O
R7	I/O	I/O	I/O
R8	I/O	I/O	I/O
R9	HCLK	HCLK	HCLK
R10	I/O	I/O	QCLKB
R11	I/O	I/O	I/O
R12	I/O	I/O	I/O
R13	I/O	I/O	I/O
R14	I/O	I/O	I/O
R15	GND	GND	GND
R16	GND	GND	GND
T1	GND	GND	GND
T2	I/O	I/O	I/O
T3	I/O	I/O	I/O
T4	NC	I/O	I/O
T5	I/O	I/O	I/O
T6	I/O	I/O	I/O
T7	I/O	I/O	I/O
T8	I/O	I/O	I/O
T9	V _{CCA}	V _{CCA}	V _{CCA}
T10	I/O	I/O	I/O
T11	I/O	I/O	I/O
T12	NC	I/O	I/O
T13	I/O	I/O	I/O
T14	I/O	I/O	I/O
T15	TDO, I/O	TDO, I/O	TDO, I/O
T16	GND	GND	GND

Package Pin Assignments (Continued)

484-Pin FBGA (Top View)



484-Pin FBGA

Pin Number	A54SX32A Function	A54SX72A Function	Pin Number	A54SX32A Function	A54SX72A Function	Pin Number	A54SX32A Function	A54SX72A Function
A1	NC*	NC	AB11	I/O	I/O	AD5	I/O	I/O
A2	NC*	NC	AB12	PRB, I/O	PRB, I/O	AD6	I/O	I/O
A3	NC*	I/O	AB13	V _{CCA}	V _{CCA}	AD7	I/O	I/O
A4	NC*	I/O	AB14	I/O	I/O	AD8	I/O	I/O
A5	NC*	I/O	AB15	I/O	I/O	AD9	V _{CCI}	V _{CCI}
A6	I/O	I/O	AB16	I/O	I/O	AD10	I/O	I/O
A7	I/O	I/O	AB17	I/O	I/O	AD11	I/O	I/O
A8	I/O	I/O	AB18	I/O	I/O	AD12	I/O	I/O
A9	I/O	I/O	AB19	I/O	I/O	AD13	V _{CCI}	V _{CCI}
A10	I/O	I/O	AB20	TDO, I/O	TDO, I/O	AD14	I/O	I/O
A11	NC*	I/O	AB21	GND	GND	AD15	I/O	I/O
A12	NC*	I/O	AB22	NC*	I/O	AD16	I/O	I/O
A13	I/O	I/O	AB23	I/O	I/O	AD17	V _{CCI}	V _{CCI}
A14	NC*	NC	AB24	I/O	I/O	AD18	I/O	I/O
A15	NC*	I/O	AB25	NC*	I/O	AD19	I/O	I/O
A16	NC*	I/O	AB26	NC*	I/O	AD20	I/O	I/O
A17	I/O	I/O	AC1	I/O	I/O	AD21	I/O	I/O
A18	I/O	I/O	AC2	I/O	I/O	AD22	I/O	I/O
A19	I/O	I/O	AC3	I/O	I/O	AD23	V _{CCI}	V _{CCI}
A20	I/O	I/O	AC4	NC*	I/O	AD24	NC*	I/O
A21	NC*	I/O	AC5	V _{CCI}	V _{CCI}	AD25	NC*	I/O
A22	NC*	I/O	AC6	I/O	I/O	AD26	NC*	I/O
A23	NC*	I/O	AC7	V _{CCI}	V _{CCI}	AE1	NC*	NC
A24	NC*	I/O	AC8	I/O	I/O	AE2	I/O	I/O
A25	NC*	NC	AC9	I/O	I/O	AE3	NC*	I/O
A26	NC*	NC	AC10	I/O	I/O	AE4	NC*	I/O
AA1	NC*	I/O	AC11	I/O	I/O	AE5	NC*	I/O
AA2	NC*	I/O	AC12	I/O	QCLKA	AE6	NC*	I/O
AA3	V _{CCA}	V _{CCA}	AC13	I/O	I/O	AE7	I/O	I/O
AA4	I/O	I/O	AC14	I/O	I/O	AE8	I/O	I/O
AA5	I/O	I/O	AC15	I/O	I/O	AE9	I/O	I/O
AA22	I/O	I/O	AC16	I/O	I/O	AE10	I/O	I/O
AA23	I/O	I/O	AC17	I/O	I/O	AE11	NC*	I/O
AA24	I/O	I/O	AC18	I/O	I/O	AE12	I/O	I/O
AA25	NC*	I/O	AC19	I/O	I/O	AE13	I/O	I/O
AA26	NC*	I/O	AC20	V _{CCI}	V _{CCI}	AE14	I/O	I/O
AB1	NC*	NC	AC21	I/O	I/O	AE15	NC*	I/O
AB2	V _{CCI}	V _{CCI}	AC22	I/O	I/O	AE16	NC*	I/O
AB3	I/O	I/O	AC23	NC*	I/O	AE17	I/O	I/O
AB4	I/O	I/O	AC24	I/O	I/O	AE18	I/O	I/O
AB5	NC*	I/O	AC25	NC*	I/O	AE19	I/O	I/O
AB6	I/O	I/O	AC26	NC*	I/O	AE20	I/O	I/O
AB7	I/O	I/O	AD1	I/O	I/O	AE21	NC*	I/O
AB8	I/O	I/O	AD2	I/O	I/O	AE22	NC*	I/O
AB9	I/O	I/O	AD3	GND	GND	AE23	NC*	I/O
AB10	I/O	I/O	AD4	I/O	I/O	AE24	NC*	I/O

Note: *These pins must be left floating on the A54SX32A device.

484-Pin FBGA (Continued)

Pin Number	A54SX32A Function	A54SX72A Function	Pin Number	A54SX32A Function	A54SX72A Function	Pin Number	A54SX32A Function	A54SX72A Function
AE25	NC*	NC	B19	I/O	I/O	D13	I/O	I/O
AE26	NC*	NC	B20	I/O	I/O	D14	I/O	I/O
AF1	NC*	NC	B21	NC*	I/O	D15	I/O	I/O
AF2	NC*	NC	B22	NC*	I/O	D16	I/O	I/O
AF3	NC	I/O	B23	NC*	I/O	D17	I/O	I/O
AF4	NC*	I/O	B24	NC*	I/O	D18	I/O	I/O
AF5	NC*	I/O	B25	I/O	I/O	D19	I/O	I/O
AF6	NC*	I/O	B26	NC*	NC	D20	I/O	I/O
AF7	I/O	I/O	C1	NC*	I/O	D21	V _{CCI}	V _{CCI}
AF8	I/O	I/O	C2	NC*	I/O	D22	GND	GND
AF9	I/O	I/O	C3	NC*	I/O	D23	I/O	I/O
AF10	I/O	I/O	C4	NC*	I/O	D24	I/O	I/O
AF11	NC*	I/O	C5	I/O	I/O	D25	NC*	I/O
AF12	NC*	NC	C6	V _{CCI}	V _{CCI}	D26	NC*	I/O
AF13	HCLK	HCLK	C7	I/O	I/O	E1	NC*	I/O
AF14	I/O	QCLKB	C8	I/O	I/O	E2	NC*	I/O
AF15	NC*	I/O	C9	V _{CCI}	V _{CCI}	E3	I/O	I/O
AF16	NC*	I/O	C10	I/O	I/O	E4	I/O	I/O
AF17	I/O	I/O	C11	I/O	I/O	E5	GND	GND
AF18	I/O	I/O	C12	I/O	I/O	E6	TDI, IO	TDI, IO
AF19	I/O	I/O	C13	PRA, I/O	PRA, I/O	E7	I/O	I/O
AF20	NC*	I/O	C14	I/O	I/O	E8	I/O	I/O
AF21	NC*	I/O	C15	I/O	QCLKD	E9	I/O	I/O
AF22	NC*	I/O	C16	I/O	I/O	E10	I/O	I/O
AF23	NC*	I/O	C17	I/O	I/O	E11	I/O	I/O
AF24	NC*	I/O	C18	I/O	I/O	E12	I/O	I/O
AF25	NC*	NC	C19	I/O	I/O	E13	V _{CCA}	V _{CCA}
AF26	NC*	NC	C20	V _{CCI}	V _{CCI}	E14	CLKB	CLKB
B1	NC*	NC	C21	I/O	I/O	E15	I/O	I/O
B2	NC*	NC	C22	I/O	I/O	E16	I/O	I/O
B3	NC*	I/O	C23	I/O	I/O	E17	I/O	I/O
B4	NC*	I/O	C24	I/O	I/O	E18	I/O	I/O
B5	NC*	I/O	C25	NC*	I/O	E19	I/O	I/O
B6	I/O	I/O	C26	NC*	I/O	E20	I/O	I/O
B7	I/O	I/O	D1	NC*	I/O	E21	I/O	I/O
B8	I/O	I/O	D2	TMS	TMS	E22	I/O	I/O
B9	I/O	I/O	D3	I/O	I/O	E23	I/O	I/O
B10	I/O	I/O	D4	V _{CCI}	V _{CCI}	E24	I/O	I/O
B11	NC*	I/O	D5	NC*	I/O	E25	V _{CCI}	V _{CCI}
B12	NC*	I/O	D6	TCK, I/O	TCK, I/O	E26	GND	GND
B13	V _{CCI}	V _{CCI}	D7	I/O	I/O	F1	V _{CCI}	V _{CCI}
B14	CLKA	CLKA	D8	I/O	I/O	F2	NC*	I/O
B15	NC*	I/O	D9	I/O	I/O	F3	NC*	I/O
B16	NC*	I/O	D10	I/O	I/O	F4	I/O	I/O
B17	I/O	I/O	D11	I/O	I/O	F5	I/O	I/O
B18	V _{CCI}	V _{CCI}	D12	I/O	QCLKC	F22	I/O	I/O

Note: *These pins must be left floating on the A54SX32A device.

484-Pin FBGA (Continued)

Pin Number	A54SX32A Function	A54SX72A Function	Pin Number	A54SX32A Function	A54SX72A Function	Pin Number	A54SX32A Function	A54SX72A Function
F23	I/O	I/O	K17	GND	GND	N5	I/O	I/O
F24	I/O	I/O	K22	I/O	I/O	N10	GND	GND
F25	I/O	I/O	K23	I/O	I/O	N11	GND	GND
F26	NC*	I/O	K24	NC*	NC	N12	GND	GND
G1	NC*	I/O	K25	NC*	I/O	N13	GND	GND
G2	NC*	I/O	K26	NC*	I/O	N14	GND	GND
G3	NC*	I/O	L1	NC*	I/O	N15	GND	GND
G4	I/O	I/O	L2	NC*	I/O	N16	GND	GND
G5	I/O	I/O	L3	I/O	I/O	N17	GND	GND
G22	I/O	I/O	L4	I/O	I/O	N22	V _{CCA}	V _{CCA}
G23	V _{CCA}	V _{CCA}	L5	I/O	I/O	N23	I/O	I/O
G24	I/O	I/O	L10	GND	GND	N24	I/O	I/O
G25	NC*	I/O	L11	GND	GND	N25	I/O	I/O
G26	NC*	I/O	L12	GND	GND	N26	NC*	NC
H1	NC*	I/O	L13	GND	GND	P1	NC*	I/O
H2	NC*	I/O	L14	GND	GND	P2	NC*	I/O
H3	I/O	I/O	L15	GND	GND	P3	I/O	I/O
H4	I/O	I/O	L16	GND	GND	P4	I/O	I/O
H5	I/O	I/O	L17	GND	GND	P5	V _{CCA}	V _{CCA}
H22	I/O	I/O	L22	I/O	I/O	P10	GND	GND
H23	I/O	I/O	L23	I/O	I/O	P11	GND	GND
H24	I/O	I/O	L24	I/O	I/O	P12	GND	GND
H25	NC*	I/O	L25	I/O	I/O	P13	GND	GND
H26	NC*	I/O	L26	I/O	I/O	P14	GND	GND
J1	NC*	I/O	M1	NC*	NC	P15	GND	GND
J2	NC*	I/O	M2	I/O	I/O	P16	GND	GND
J3	I/O	I/O	M3	I/O	I/O	P17	GND	GND
J4	I/O	I/O	M4	I/O	I/O	P22	I/O	I/O
J5	I/O	I/O	M5	I/O	I/O	P23	I/O	I/O
J22	I/O	I/O	M10	GND	GND	P24	V _{CCI}	V _{CCI}
J23	I/O	I/O	M11	GND	GND	P25	I/O	I/O
J24	I/O	I/O	M12	GND	GND	P26	I/O	I/O
J25	V _{CCI}	V _{CCI}	M13	GND	GND	R1	NC*	I/O
J26	NC*	I/O	M14	GND	GND	R2	NC*	I/O
K1	I/O	I/O	M15	GND	GND	R3	I/O	I/O
K2	V _{CCI}	V _{CCI}	M16	GND	GND	R4	I/O	I/O
K3	I/O	I/O	M17	GND	GND	R5	TRST, I/O	TRST, I/O
K4	I/O	I/O	M22	I/O	I/O	R10	GND	GND
K5	V _{CCA}	V _{CCA}	M23	I/O	I/O	R11	GND	GND
K10	GND	GND	M24	I/O	I/O	R12	GND	GND
K11	GND	GND	M25	NC*	I/O	R13	GND	GND
K12	GND	GND	M26	NC*	I/O	R14	GND	GND
K13	GND	GND	N1	I/O	I/O	R15	GND	GND
K14	GND	GND	N2	V _{CCI}	V _{CCI}	R16	GND	GND
K15	GND	GND	N3	I/O	I/O	R17	GND	GND
K16	GND	GND	N4	I/O	I/O	R22	I/O	I/O

Note: *These pins must be left floating on the A54SX32A device.

484-Pin FBGA (Continued)

Pin Number	A54SX32A Function	A54SX72A Function
R23	I/O	I/O
R24	I/O	I/O
R25	NC*	I/O
R26	NC*	I/O
T1	NC*	I/O
T2	NC*	I/O
T3	I/O	I/O
T4	I/O	I/O
T5	I/O	I/O
T10	GND	GND
T11	GND	GND
T12	GND	GND
T13	GND	GND
T14	GND	GND
T15	GND	GND
T16	GND	GND
T17	GND	GND
T22	I/O	I/O
T23	I/O	I/O
T24	I/O	I/O
T25	NC*	I/O
T26	NC*	I/O
U1	I/O	I/O
U2	V _{CCI}	V _{CCI}

Pin Number	A54SX32A Function	A54SX72A Function
U3	I/O	I/O
U4	I/O	I/O
U5	I/O	I/O
U10	GND	GND
U11	GND	GND
U12	GND	GND
U13	GND	GND
U14	GND	GND
U15	GND	GND
U16	GND	GND
U17	GND	GND
U22	I/O	I/O
U23	I/O	I/O
U24	I/O	I/O
U25	V _{CCI}	V _{CCI}
U26	I/O	I/O
V1	NC*	I/O
V2	NC*	I/O
V3	I/O	I/O
V4	I/O	I/O
V5	I/O	I/O
V22	V _{CCA}	V _{CCA}
V23	I/O	I/O
V24	I/O	I/O

Pin Number	A54SX32A Function	A54SX72A Function
V25	NC*	I/O
V26	NC*	I/O
W1	I/O	I/O
W2	I/O	I/O
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W22	I/O	I/O
W23	V _{CCA}	V _{CCA}
W24	I/O	I/O
W25	NC*	I/O
W26	NC*	I/O
Y1	NC*	I/O
Y2	NC*	I/O
Y3	I/O	I/O
Y4	I/O	I/O
Y5	NC*	I/O
Y22	I/O	I/O
Y23	I/O	I/O
Y24	V _{CCI}	V _{CCI}
Y25	I/O	I/O
Y26	I/O	I/O

Note: *These pins must be left floating on the A54SX32A device.

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous version	Changes in current version (v3.0)	Page
v4.0	The “SX-A Product Profile” table on page 1 was updated.	page 1
	The “Ordering Information” section on page 2 was updated.	page 2
	The “Product Plan” section on page 3 was updated.	page 3
	Figure 1 on page 4 was updated.	page 4
	The “Clock Resources” section on page 6 was updated.	page 6
	The “SX-A Clock Resources” table on page 8 is new.	page 8
	The “User Security” section on page 9 is new.	page 9
	The “I/O Modules” section on page 9 was updated.	page 9
	The “I/O Features” table on page 10 was updated.	page 10
	The “I/O Characteristics for All I/O Configurations” table on page 10 is new.	page 10
	The “Power-up Time at which I/Os Become Active” table on page 10 is new.	page 10
	Figure 10 on page 11 is new.	page 11
	The “Boundary-Scan Pin Configurations and Functions” table on page 11 is new.	page 11
	The “Device Configuration Options for Probe Capability (TRST pin reserved)” table on page 12 is new.	page 12
	The “SX-A Probe Circuit Control Pins” section on page 12 was updated.	page 12
	The “Design Considerations” section on page 12 was updated.	page 12
	Figure 11 on page 12 was updated.	page 12
	The “Development Tool Support” section on page 13 was updated.	page 13
	Figure 12 on page 13 is new.	page 13
	The “Absolute Maximum Ratings1” table on page 14 was updated.	page 14
The “Recommended Operating Conditions” table on page 14 was updated.	page 14	
The “3.3V LVTTTL and 5V TTL Electrical Specifications” table on page 14 was updated.	page 14	
The “2.5V LVCMOS2 Electrical Specifications” table on page 15 was updated.	page 15	
The SX-A Timing Model* and Sample Path Calculations equations were updated.	page 22	
The “Pin Description” section on page 53 was updated.	page 53	
v2.0.1	The section, “Development Tool Support” section on page 13 has been updated.	page 10
	The section, “I/O Modules” section on page 9, and the table, I/O Features, Table 2 on page 10 have been updated.	page 9
	The “SX-A Timing Model*” section on page 22 and several timing tables on pages 22-49 have new timing numbers.	pages 19, 22-49

Data Sheet Categories

In order to provide the latest information to designers, some data sheets are published before data has been fully characterized. These data sheets are marked as “Advanced” or Preliminary” data sheets. The definition of these categories are as follows:

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